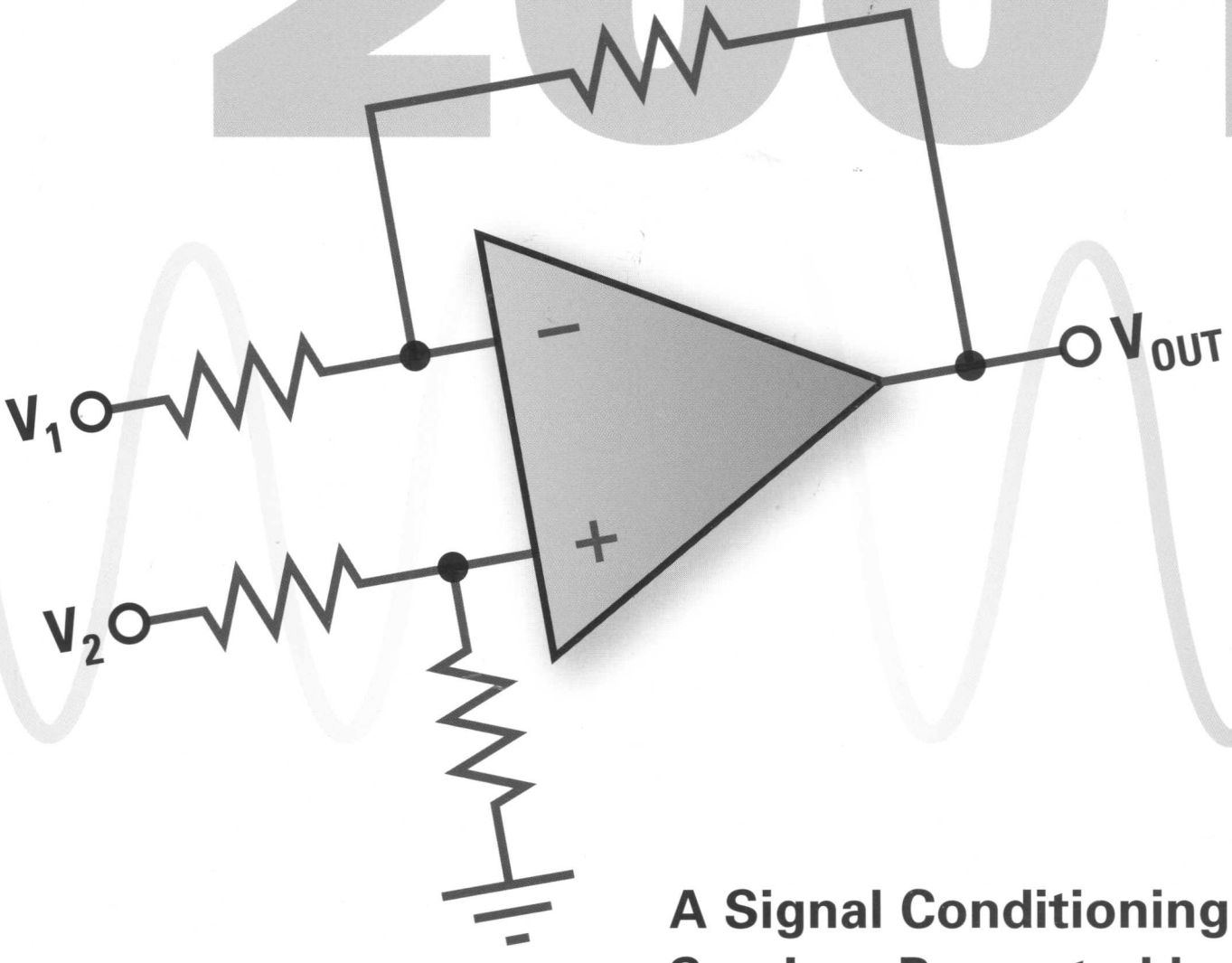
AK.

Building the Analog Tool Kit

2001



A Signal Conditioning Seminar Presented by Texas Instruments.

BB Burr-Brown Products from Texas Instruments

Section 1

1-16 Notes: change the formula for phase angle to

$$\theta = -\tan^{-1}\left(\frac{\omega\tau}{1}\right)$$

Change text to read "the tangent of 90 deg is infinity"

1-23 Changed graph labels to -20dB/Decade and -40dB/decade

1-26 Correct location of dotted lines on graph. (Moved location of 1/T1 and 1/T2)

1-32 Top graph, show some undershoot as well.

1-56 Move location of current arrow in input model.

1-69 Changed table label from "Ideal Loop Gain" to "Loop Gain"

Section 2a

2-4 left side of schematic, change Vout to Vref.

2-8 thru 2-15 change term mVin

2-20 Moved breakpoint of relative THD and changed TDH to THD

2-25 add missing formula adjust reflection coefficient formulas.

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_F + R_G}{R_F}\left(\frac{R_T}{R_H + R_T}\right)$$

2-40 Added "Amplitude Sensitive Applications" to text box

2-41 Added "Frequency Sensitive Applications" to text box

2-42 Added "Harmonic Sensitive Applications" to text box

2-43 Added a text box that says "Preserves Signal Frequency Structure"

2-57 Changed the formula for V(OUTMAX)

$$V_{OUTMAX} = V_{OH(MIN)} - V_{OL(MAX)}$$

2-60 swap columns for units and OPA340

Section 2b

2-77 Change units on Iq/Amp section to microamps.

Section 3

3-3 This slide has a grammatical error in the text. Deleted the word "reference" 3 line from last.

3-8 change typographical errors kW to k ohm and VOS to Vos.

3-9 Rout row, inserted 20 k ohm in blank

3-11 change total error from 18 to 96 LSB

3-12 change m to micro.

Section 4

4-12 and 13: these figures do not match the text. The text describes a follower amplifier used as a buffer for Vref. Two slides added. Existing text moved to slides 4-14 and 4-15. Added circuit description text to 4-12. 4-14 is the schematic and 4-15 the curve.

Section 5 - Appendix 1

Added extra slides to show new amplifiers tools available on the web.

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A Signal Conditioning Seminar

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Section 2. Adding New Circuit Design Tools

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Break

Section 4 Communications Sensor to ADC Design

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Wrap up

Section 1

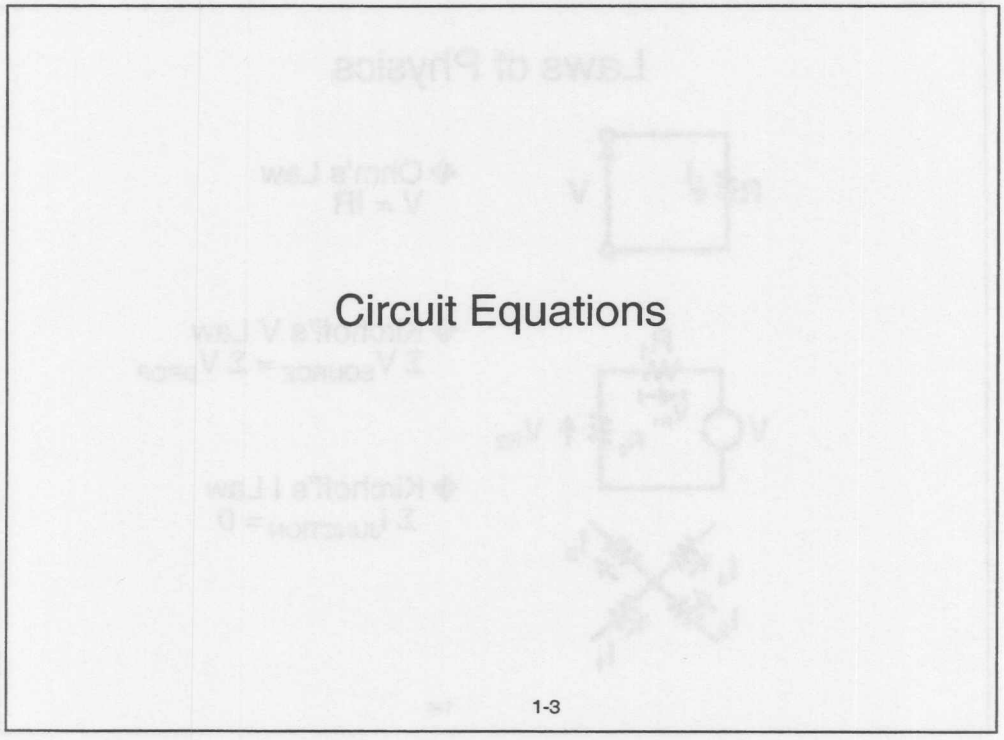
Sharpening The Fundamental Tools

1-1

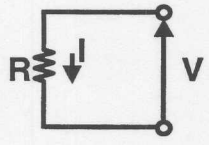
Sharpening the Fundamental Tools

- Circuit Equations
- Bode Plots
- Stability
- Voltage Feedback Equations
- Voltage Feedback Compensation
- Current Feedback Equations
- CFB versus VFB

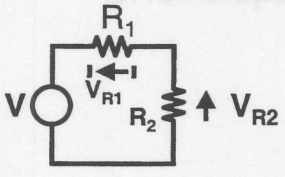
1-2


Circuit Equations
1-3

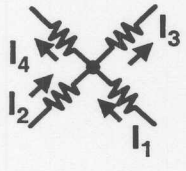
Laws of Physics



◆ Ohm's Law
$V = IR$



◆ Kirchoff's V Law
$\Sigma V_{SOURCE} = \Sigma V_{DROP}$



◆ Kirchoff's I Law
$\Sigma I_{JUNCTION} = 0$

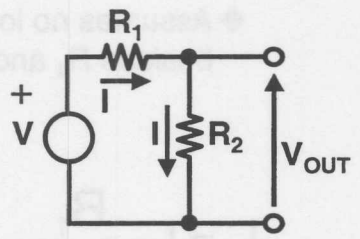
1-4

Ohm's law, V=IR, is fundamental to all electronics. It can be applied to a single component or to a complete circuit. When the current flowing through any portion of a circuit is known, the voltage dropped across that portion of the circuit is obtained by multiplying the current times the resistance.

Kirchoff's voltage law states that the sum of the voltage drops in a series circuit equals the sum of the voltage sources. When taking sums keep in mind that the sum is an algebraic quantity.

Kirchoff's current law states: the sum of the currents entering a junction equal the sum of the currents leaving a junction. It makes no difference if a current comes from a current source or through a resistor because all currents are treated equal.

Voltage Divider Rule



◆ Assumes that R_2 is not loaded

$$V_{OUT} = V\frac{R_2}{R_1 + R_2}$$

$$V = IR_1 + IR_2 = I(R_1 + R_2)$$

$$I = \frac{V}{(R_1 + R_2)}$$

$$V_{OUT} = IR_2 = \frac{V}{(R_1 + R_2)}(R_2) = V\frac{R_2}{R_1 + R_2}$$

1-5

When the output of a circuit is not loaded, the voltage divider rule can be used to calculate the circuit's output voltage. Assume that the same current flows through all circuit elements. Equation 1-1 is written using Ohm's law. Algebraic manipulation yields equation 1-2:

$$V = I(R_1 + R_2) \quad (1\text{-}1)$$

$$I = \frac{V}{(R_1 + R_2)} \quad (1\text{-}2)$$

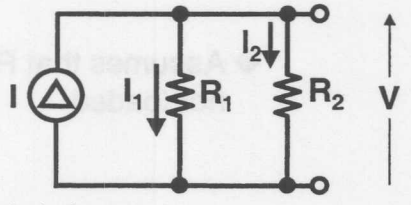
Again, Ohm's law is used on the output circuit yielding equation 1-3. Substituting equation 1-2 into 1-3 yields equation 1-4:

$$V_{OUT} = IR_2 \quad (1\text{-}3)$$

$$V_{OUT} = V\frac{R_2}{R_1 + R_2} \quad (1\text{-}4)$$

The output resistor is divided by the total circuit resistance, and this fraction is multiplied by the input voltage to obtain the output voltage. Output resistor divided by the total resistance is a simple way to remember the voltage divider rule.

Current Divider Rule



◆ Assumes no load besides R_1 and R_2

$$I_2 = I\frac{R_1}{R_1 + R_2}$$

$I = I_1 + I_2$

$V = I_1R_1 = I_2R_2$

$I_1 = I_2\frac{R_2}{R_1}$

$I = I_1 + I_2 = I_2\frac{R_2}{R_1} + I_2 = I_2\left(1 + \frac{R_2}{R_1}\right) = I_2\left(\frac{R_1 + R_2}{R_1}\right)$

Then: $I_2 = I\frac{R_1}{R_1 + R_2}$

1-6

When the output of a circuit is not loaded, the current divider rule can be used to calculate the current flow in the output component. The currents I_1 and I_2 are assumed to be flowing in the branch circuit. Equation 1-5 is written with the aid of Kirchoff's current law. The circuit voltage is written in equation 1-6 with the aid of Ohm's law. Combining equations 1-5 and 1-6 yields equation 1-7:

$$I = I_1 + I_2 \quad (1\text{-}5)$$

$$V = I_1R_1 = I_2R_2 \quad (1\text{-}6)$$

$$I = I_1 + I_2 = I_2\left(\frac{R_2}{R_1}\right) + I_2 = I_2\left(1 + \frac{R_2}{R_1}\right) = I_2\left(\frac{R_1 + R_2}{R_1}\right) \quad (1\text{-}7)$$

Rearranging the terms in equation 1-7 yields equation 1-8:

$$I_2 = I\frac{R_1}{R_1 + R_2} \quad (1\text{-}8)$$

The total circuit current divides into two parts, and the resistance, R_1, divided by the total resistance determines how much current flows through R_2. A way to remember the current divider rule is that the opposite resistor is divided by the total resistance.

Thevenin's and Norton's Theorems

- Employed to isolate some part of the circuit
- Results in a simplified equivalent circuit
- Much quicker analysis
- If input is a voltage source use Thevenin's theorem
- If input is a current source use Norton's theorem

1-7

There are times when it is advantageous to isolate a part of the circuit. Rather than write loop or node equations and solving them simultaneously, Thevenin's theorem enables us to isolate the part of the circuit we are interested in. We replace the remaining circuit with a simple series equivalent circuit, thus Thevenin's theorem simplifies the analysis.

There are two theorems that do similar functions, and the second theorem is called Norton's theorem. Thevenin's theorem is used when the input is a voltage source, and Norton's theorem is used when the input is a current source. Norton's theorem is rarely used, so its explanation is left to outside sources.

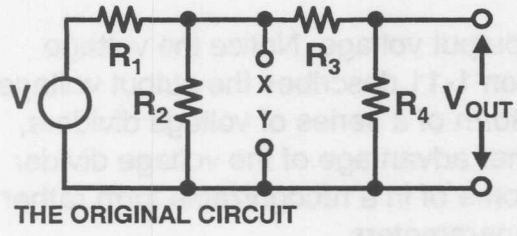
Calculating Thevenin's Theorem

- Look into the terminals of the components being replaced
- Calculate the no load open circuit voltage
- Short independent voltage sources, open independent current sources
- Calculate the impedance
- Replace original circuit with Thevenin

The rules for Thevenin's theorem start with the component or part of the circuit being replaced. Look into the terminals of the circuit being replaced, and calculate the no load voltage as seen from these terminals (much like calculating a voltage divider). Again, looking into the terminals of the circuit being replaced, short independent voltage sources, and calculate the impedance between these terminals. Now, the next step is to substitute the Thevenin equivalent circuit for the circuit part you wanted to replace.

The Thevenin equivalent circuit is a simple series circuit; thus further calculations are simplified. The simplification of circuit calculations is often sufficient reason to use Thevenin's theorem because it eliminates the need for solving several simultaneous equations. The detailed information about what happens in the circuit that was replaced is not available when using Thevenin's theorem, but that is of no consequence because you had no interest in it.

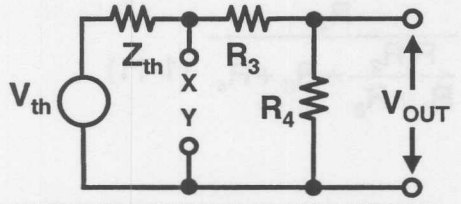
Thevenin Theorem Example



THE ORIGINAL CIRCUIT

$$V_{th} = V\frac{R_2}{R_1 + R_2}$$

$$R_{th} = R_{x-y} = \frac{R_1 R_2}{R_1 + R_2} \equiv R_1 \| R_2$$



THE THEVENIN EQUIVALENT CIRCUIT

$$V_{OUT} = V_{th}\frac{R_4}{Z_{th} + R_3 + R_4}$$

$$= V\frac{R_2}{R_1 + R_2}\frac{R_4}{\frac{R_1 R_2}{R_1 + R_2} + R_3 + R_4}$$

1-9

In this example we want to calculate the output voltage, V_O. The first step is to stand on the terminals X-Y with your back to the output circuit, and calculate the open circuit voltage seen. This is a perfect opportunity to use the voltage divider rule to obtain equation 1-9.

$$V_{th} = V\frac{R_2}{R_1 + R_2} \quad (1\text{-}9)$$

Still standing on the terminals X-Y, step two is to calculate the impedance seen looking into these terminals with V shorted. The Thevenin impedance is the parallel impedance of R_1 and R_2 as calculated in equation 1-10.

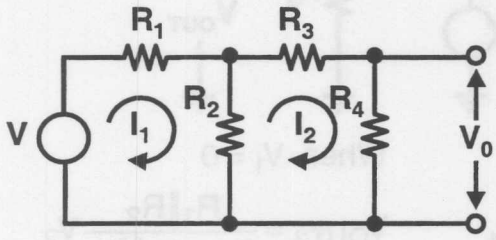
$$Z_{th} = Z_{x-y} = \frac{R_1 R_2}{R_1 + R_2} \equiv R_1 \| R_2 \quad (1\text{-}10)$$

Now get off the terminals X-Y before you damage them with your big feet. Step three replaces the circuit to the left of X-Y with the Thevenin equivalent circuit V_{th} and R_{th}.

The final step is to calculate the output voltage. Notice the voltage divider rule is used again. Equation 1-11 describes the output voltage, and it comes out naturally in the form of a series of voltage dividers, which makes sense. That's another advantage of the voltage divider rule; that the answers normally come of in a recognizable form rather than a jumble of coefficients and parameters.

$$V_0 = V_{th}\frac{R_4}{Z_{th}+R_3+R_4} = V\frac{R_2}{R_1+R_2}\frac{R_4}{\frac{R_1R_2}{R_1+R_2}+R_3+R_4} \quad (1\text{-}11)$$

Doing the Analysis the Hard Way



$$V = I_1(R_1 + R_2) - I_2R_2$$

$$I_2(R_2 + R_3 + R_4) = I_1R_2$$

$$I_1 = \frac{R_2 + R_3 + R_4}{R_2} I_2$$

$$V = I_2 \frac{(R_2 + R_3 + R_4)}{R_2}(R_1 + R_2) - I_2R_2$$

$$I_2 = \frac{V}{\frac{R_2 + R_3 + R_4}{R_2}(R_1 + R_2) - R_2}$$

$$V_{OUT} = I_2R_4$$

$$V_{OUT} = V \frac{R_4}{\frac{(R_2 + R_3 + R_4)(R_1 + R_2)}{R_2} - R_2}$$

The circuit analysis is done here the hard way so you can see the advantage of using Thevenin's Theorem. Two loop currents, I_1 and I_2, are assigned to the circuit. Then the loop equations, 1-12 and 1-13, are written. Equation 1-13 is rewritten in equation 1-14, and substituted into equation 1-12. The terms are rearranged in equation 1-16. Ohm's law is used to write equation 1-17, and the final substitutions are made in equation 1-18.

This is a lot of extra work for no gain. Also, the answer is not in a usable form, thus more algebra is required to get the answer into usable form.

$$V = I_1(R_1 + R_2) - I_2R_2 \quad (1\text{-}12)$$

$$I_2(R_2 + R_3 + R_4) = I_1R_2 \quad (1\text{-}13)$$

$$I_1 = \frac{R_2 + R_3 + R_4}{R_2} I_2 \quad (1\text{-}14)$$

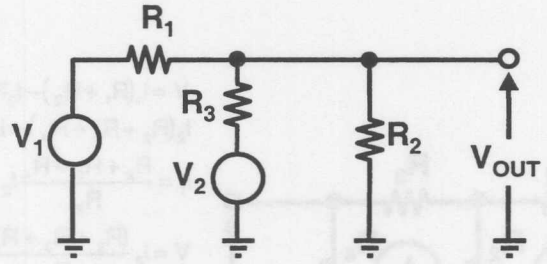
$$V = I_2 \frac{(R_2 + R_3 + R_4)}{R_2}(R_1 + R_2) - I_2R_2 \quad (1\text{-}15)$$

$$I_2 = \frac{V}{\frac{R_2 + R_3 + R_4}{R_2}(R_1 + R_2) - R_2} \quad (1\text{-}16)$$

$$V_0 = I_2R_4 \quad (1\text{-}17)$$

$$V_0 = V \frac{R_4}{\frac{(R_2 + R_3 + R_4)(R_1 + R_2)}{R_2} - R_2} \quad (1\text{-}18)$$

Superposition Example



When $V_2 = 0$

$$V_{OUT1} = \frac{R_2 \| R_3}{R_1 + R_2 \| R_3} V_1$$

When $V_1 = 0$

$$V_{OUT2} = \frac{R_1 \| R_2}{R_3 + R_1 \| R_2} V_2$$

$$V_{OUT} = V_{OUT1} + V_{OUT2} = V_1 \frac{R_2 \| R_3}{R_1 + R_2 \| R_3} + V_2 \frac{R_1 \| R_2}{R_3 + R_1 \| R_2}$$

Superposition is a theorem that can be applied to any linear circuit. Essentially, when there are independent sources, the voltages and currents resulting from each source can be calculated separately, and the results are added algebraically. This simplifies the calculations because it keeps from having to write a series of loop or node equations.

When $V_2 = 0$ or is grounded, V_1 forms a voltage divider with R_1 and the parallel combination of R_2 and R_3. The voltage divider theorem yields the answer quickly. Likewise, when $V_1 = 0$, V_2 forms a voltage divider with R_3 and the parallel combination of R_1 and R_2, and the voltage divider theorem is applied again. After the calculations for each source are made the components are added to obtain the final solution.

The reader should analyze this circuit with loop or node equations, and then they are sure to become a fan of superposition. Again, the superposition results come out is a simple arrangement that is easy to understand. One looks at the final equation and it is obvious that if the sources are equal and opposite polarity, and $R_1 = R_3$, then the output voltage is zero. Conclusions such as this are hard to make after the results of a loop or node analysis unless considerable effort is made to manipulate the final equation into symmetrical form.

Bode Plots

1-13

Bode Plots

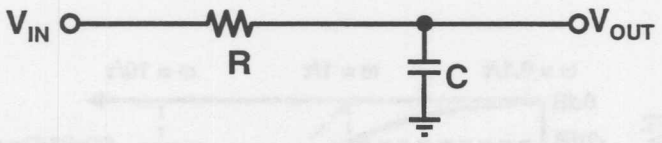
- Developed by H.W. Bode in 1945.
- Bode plots are log plots.
- Uses logs so equations can be added and subtracted graphically.
- 20Log(F(t)) = 20Log|F(t)| + Phase Angle

1-14

H. W. Bode developed a quick, accurate, and easy method of analyzing feedback amplifiers, and he published a book about his techniques in 1945. Op amps had not been developed when Bode published his book, but they fall under the general classification of feedback amplifiers, so they are easily analyzed with Bode techniques. The mathematical manipulations required to analyze a feedback circuit are complicated because they involve multiplication and division. The Bode plot simplifies the analysis through the use of graphical techniques.

The Bode equations are log equations which take the form 20Log(F(t)) = 20Log $|F(t)|$ + phase angle. Taking the log of a function breaks the function into its component parts; the magnitude and the phase. Terms that are normally multiplied and divided can now be added and subtracted because they are log equations. The addition and subtraction is done graphically, thus easing the calculations and giving the designer a pictorial representation of circuit performance.

Integrator Circuit



$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{(1+\tau s)}$$

Where $s = j\omega$, $j = \sqrt{-1}$ and $\tau = RC$

1-15

The equation for the low pass filter is written below:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1+RCs} = \frac{1}{1+\tau s} \qquad (1\text{-}19)$$

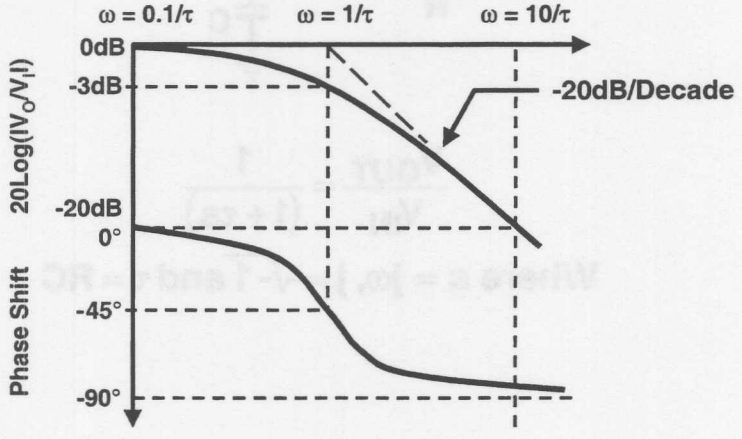
Where $\tau = RC$, and $j = \sqrt{(-1)}$

The magnitude of this transfer function is

$$|V_{OUT}/V_{IN}| = 1/\sqrt{(1+(\tau\omega)^2)} \qquad (1\text{-}20)$$

The magnitude equals $|V_{OUT}/V_{IN}| = 1$ when $\omega = 0.1/\tau$; it equals 0.707 when $\omega = 1/\tau$, and it equals 0.1 when $\omega = 10/\tau$.

Bode Plot of Integrating Circuit



1-16

These points are plotted in the figure using straight-line approximations. The negative slope is -20dB/decade or -6dB/octave. The magnitude curve is plotted as a horizontal line until it intersects the breakpoint where $\omega = 1/\tau$. The negative slope begins at the breakpoint because the magnitude decreases rapidly at that point. The gain is equal to 1 or 0dB at very low frequencies, equal to 0.707 or -3db at the break frequency, and it keeps falling with a -20db/decade slope for higher frequencies.

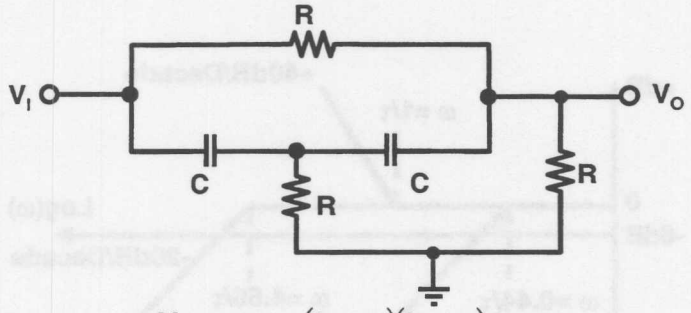
The phase shift for the low pass filter or any other transfer function is calculated as shown below:

$$\phi = \tan^{-1}\left(\frac{1}{\omega\tau}\right) \quad (1\text{-}21)$$

The phase shift is much harder to draw on a Bode plot because the tangent function is non-linear. The phase information around the 0dB intercept point yields the stability information for an active circuit, so the phase calculations are only done at the point near the 0dB crossover. The phase is approximated by remembering that the tangent of 90° is ∞, 60° is $\sqrt{3}$, of 45° is 1, and the tangent of 30° is $\sqrt{3}/3$.

A breakpoint occurring in the denominator is called a pole, and it slopes down. Conversely, a breakpoint occurring in the numerator is called a zero, and it slopes up. When the transfer function has multiple poles and zeros, each pole or zero is plotted independently, and the individual poles/zeros are added graphically. If multiple poles, zeros, or a pole/zero combination have the same breakpoint they are plotted on top of each other. Multiple poles or zeros cause the slope to change by 0dB/decade, 20dB/decade, 40db/decade, or more.

Band Reject Filter

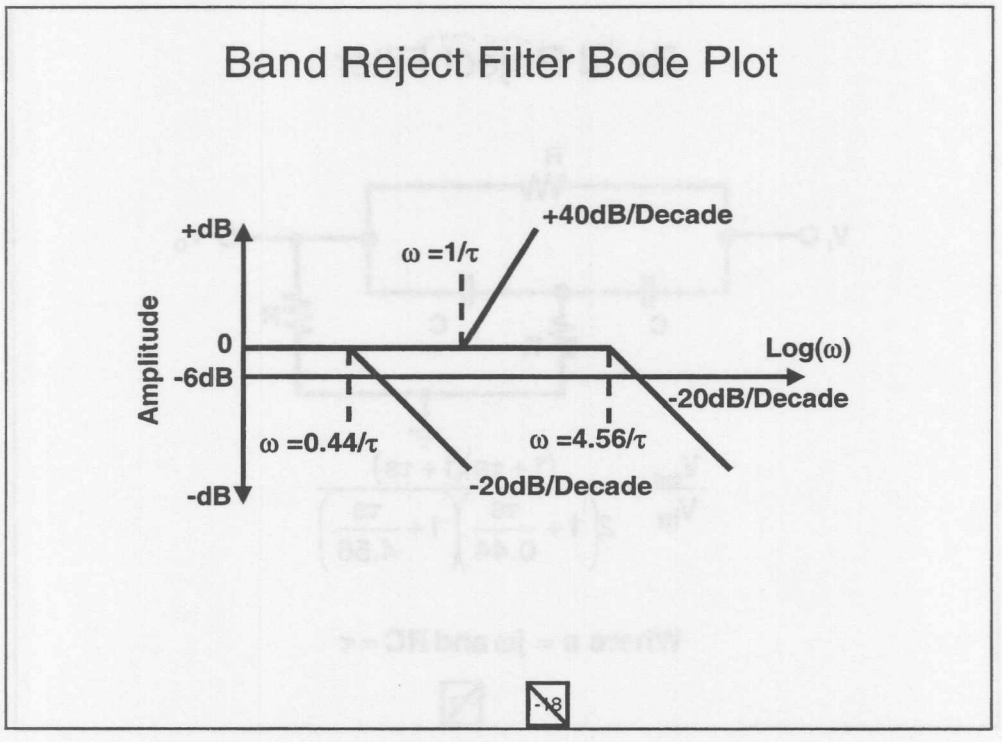


$$\frac{V_{out}}{V_{in}} = \frac{(1+\tau s)(1+\tau s)}{2\left(1+\frac{\tau s}{0.44}\right)\left(1+\frac{\tau s}{4.56}\right)}$$

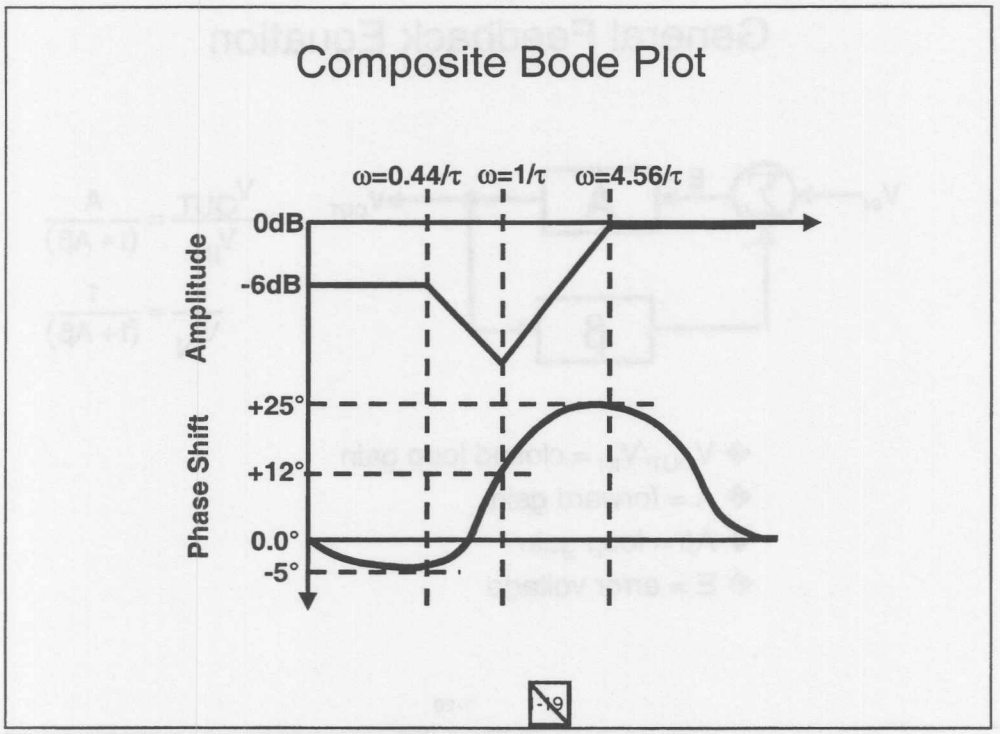
Where $s = j\omega$ and $RC = \tau$

An example of a transfer function with multiple poles and zeros is a band reject filter. The transfer function of the band reject filter is given below.

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{(1+\tau s)(1+\tau s)}{2\left(1+\frac{\tau s}{0.44}\right)\left(1+\frac{\tau s}{4.56}\right)} \qquad (1\text{-}22)$$



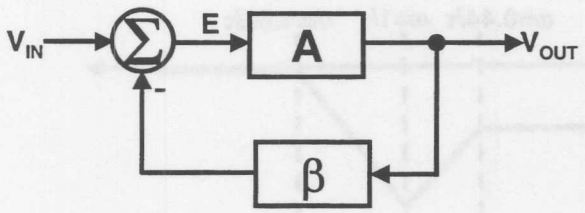
The individual plots show the dc gain of 1/2 plotting as a straight line from the –6dB intercept. The two zeros occur at the same break frequency. Thus they are plotted with a +40db/decade slope. The two poles are plotted at their breakpoints of 0.44 and 4.56, and each pole has a –20dB/decade slope.



The dc gain causes the amplitude of the combined plot to intercept the axis at -6dB, and it breaks down when it reaches the first pole, $\omega = 0.44/\tau$. When the amplitude function gets to the double zero at $\omega = 1/\tau$, the first zero cancels out the pole, and the second zero breaks up resulting in a slope of 20dB/decade. The upward slope continues until the second pole cancels out the second zero at $\omega = 4.56/\tau$, and the amplitude is flat from that point out in frequency.

When the separation between pole zero combinations is a decade or more in frequency, it is easy to draw the Bode plot because there is little interaction between the poles and/or zeros. As the poles and/or zeros get closer together the plot gets harder to make because their interaction around the break points caused by the closeness magnifies the -3dB breakpoint error. The phase is especially hard to plot because it is a tangent function, but picking a few salient points and sketching them in first gets you a pretty good approximation. The Bode plot enables the designer to get a good idea of pole zero placement, and it is valuable for fast evaluation of possible compensation techniques. When the situation gets critical, accurate calculations must be made and plotted to insure that the plot represents the true situation.

General Feedback Equation



$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{(1+A\beta)}$$

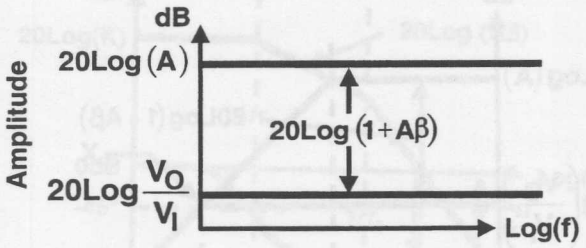
$$\frac{E}{V_{IN}} = \frac{1}{(1+A\beta)}$$

- V_{OUT}/V_{IN} = closed loop gain
- A = forward gain
- Aβ = loop gain
- E = error voltage

1-20

When Gain is Independent of Frequency

$$\frac{V_O}{V_I} = \frac{A}{1 + A\beta}$$



-21

Consider this equation:

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \qquad (1\text{-}23)$$

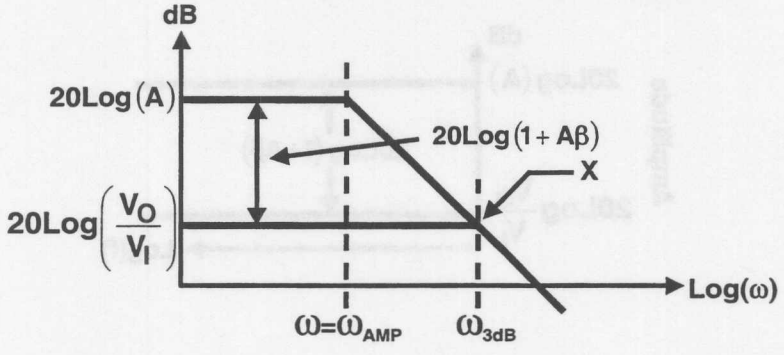
Taking the log of this equation yields:

$$20\text{Log}(V_{OUT}/V_{IN}) = 20\text{Log}|A| - 20\text{Log}|1 + A\beta| \qquad (1\text{-}24)$$

If A and β do not contain poles or zeros there are no break points. Then the Bode plot is flat, and because there are no poles or zeros to contribute phase shift, the circuit can't oscillate.

When Gain is Frequency Dependent
(Typical Single Pole Op Amp)

$$\frac{V_O}{V_I} = \frac{A}{1 + A\beta} \qquad A = \frac{a}{1 + j\frac{\omega}{\omega_{AMP}}}$$



1-22

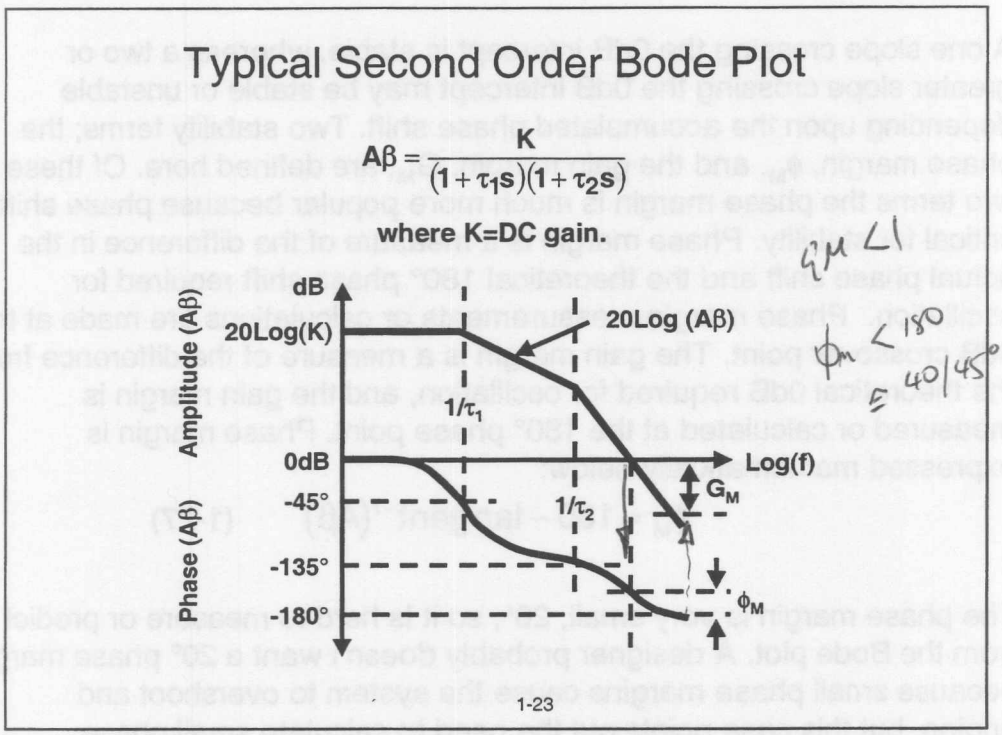
All real op amps have many poles, and some op amps have little or no internal compensation, so these op amps must be externally compensated to prevent oscillation. A different breed of op amp is internally compensated so that they appear to have a single pole. Beware, these op amps only appear to have a single pole, and at high frequencies they may accumulate as much as 155° phase shift before the gain intercepts the 0dB axis. Such an amplifier would have an approximate equation similar to that given below.

$$A = \frac{a}{1 + j\frac{\omega}{\omega_a}} \qquad (1\text{-}25)$$

The amplifier gain, A, intercepts the axis at 20Log(A), and it breaks down at a slope of - 20dB/decade at $\omega = \omega_a$. The negative slope continues for all frequencies greater than the breakpoint, $\omega = \omega_a$. The closed loop circuit gain intercepts the axis at $20\text{Log}(V_{OUT}/V_{IN})$, and because β does not have any poles or zeros, the closed loop circuit gain is constant until it's projection intersects the amplifier gain at point X. After intersection with the amplifier gain curve, the closed loop gain follows the amplifier gain because the amplifier becomes the controlling factor.

Actually, the closed loop gain starts to roll off earlier, and it is down 3dB at point X. At point X the difference between the closed loop gain and the amplifier gain is -3dB, thus the term $-20\text{Log}|1+A\beta| = -3\text{dB}$. The magnitude of 3dB is $\sqrt{2}$, hence $\sqrt{1+(A\beta)^2} = \sqrt{2}$ and elimination of the radicals shows that $A\beta = 1$.

See Errata



The loop gain transfer function is given below in a form common to many circuits, so it is analyzed in detail.

$$A\beta = \frac{K}{(1+\tau_1 s)(1+\tau_2 s)} \quad (1\text{-}26)$$

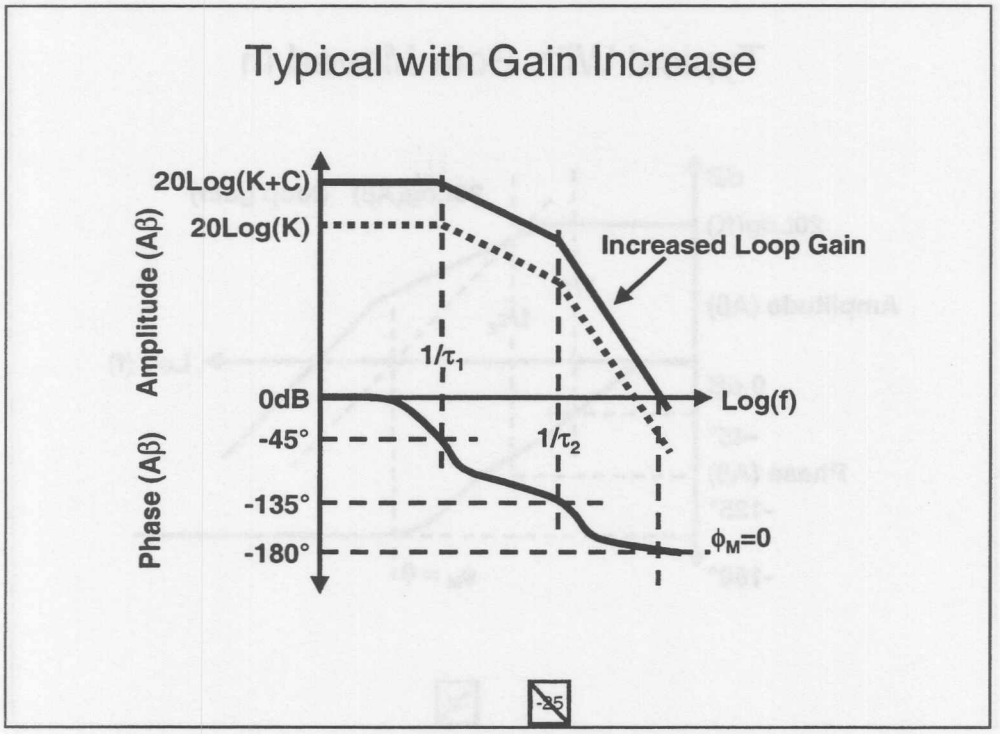
The quantity, K, is the dc gain, and it plots as a straight line with an intercept of 20Log(K). The two break points, $\omega = \omega_1$ and $\omega = \omega_2$, are plotted in the Bode plot. Each breakpoint contributes -20dB/decade slope to the plot, and 45° phase shift resulting from each breakpoint is plotted at the breakpoints.

This transfer function is referred to as a "two slope" because it has two breakpoints resulting in a - 40dB/decade slope. When a Bode plot crosses the 0dB (loop gain equals one) intercept the two slope indicates that significant phase shift has accumulated, and consequently, the circuit may meet the criteria for oscillation. Notice that a one slope can only accumulate 90° phase shift, so a one slope transfer function can't oscillate. Furthermore, a two slope system can accumulate 180° phase shift, therefore a transfer function with a two or greater slope is capable of oscillation (especially in the real world where stray capacitance may introduce a third slope).

A one slope crossing the 0dB intercept is stable, whereas a two or greater slope crossing the 0dB intercept may be stable or unstable depending upon the accumulated phase shift. Two stability terms; the phase margin, ϕ_M, and the gain margin, G_M, are defined here. Of these two terms the phase margin is much more popular because phase shift is critical for stability. Phase margin is a measure of the difference in the actual phase shift and the theoretical 180° phase shift required for oscillation. Phase margin measurements or calculations are made at the 0dB crossover point. The gain margin is a measure of the difference from the theoretical 0dB required for oscillation, and the gain margin is measured or calculated at the 180° phase point. Phase margin is expressed mathematically below:

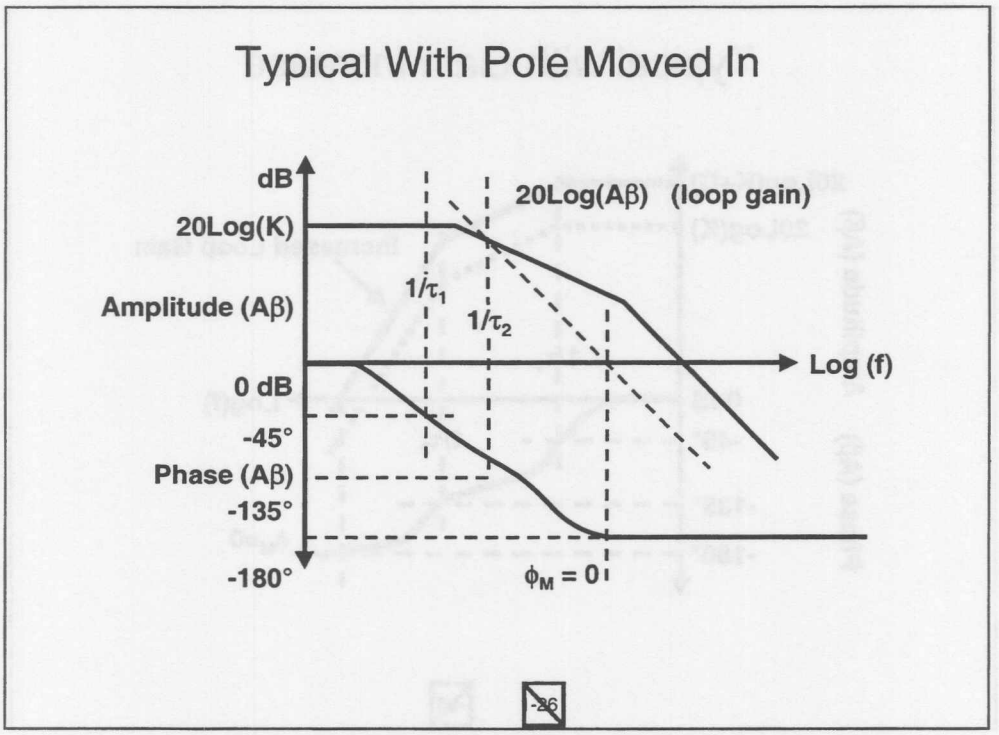
$$\phi_M = 180 - \text{tangent}^{-1}(A\beta) \qquad (1\text{-}27)$$

The phase margin is very small, 20°, so it is hard to measure or predict from the Bode plot. A designer probably doesn't want a 20° phase margin because small phase margins cause the system to overshoot and ringing, but this case points out the need to calculate small phase margins carefully. The circuit is stable, and it doesn't oscillate because the phase margin is positive. Also, the circuit with the smallest phase margin has the highest frequency response and bandwidth.



Increasing the loop gain to (K+C) shifts the loop gain magnitude plot up. The pole locations are constant, thus the 0dB crossover point moves to the right. This causes more phase shift to accumulate, and the phase margin is reduced to zero. The circuit becomes oscillatory with no phase margin, but the circuit is not good for much in this condition because production tolerances and worst case conditions insure that the circuit will oscillate when you want it to amplify, and vice versa. Remember that decreasing the closed loop gain results in an increased loop gain that decreases stability.

See Errata



When the circuit poles are spaced closer the situation results in a faster accumulation of phase shift. The phase margin is zero because the loop gain phase shift reaches 180° before the magnitude passes through 0dB. This circuit oscillates, but it is not a very stable oscillator because the transition to 180° phase shift is very slow. Stable oscillators have a very sharp transition through 180°. Remember, adding a capacitor to the circuit as people often do when they are trying to eliminate an oscillation can cause a pole to appear close in, and the added pole exacerbates the oscillation problem.

Stability

Peaking

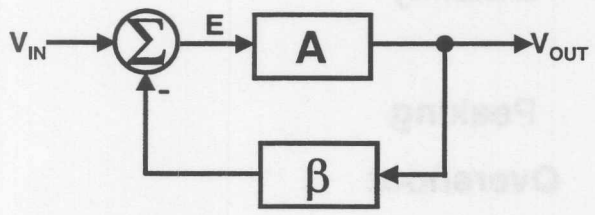
Overshoot

Ringing

Oscillation

1-27

The Feedback Equation (Circuit Theory)



$$V_{OUT} = EA$$

$$E = V_{IN} - \beta V_{OUT}$$

$$E = \frac{V_{OUT}}{A}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{(1+A\beta)}$$

$$\frac{E}{V_{IN}} = \frac{1}{(1+A\beta)}$$

-28

The output equation and error equation are written below.

$$E = V_I - \beta V_O, \quad V_{OUT} = EA \qquad (1\text{-}28)$$

Combining these equations yields;

$$\frac{V_{OUT}}{A} = V_{IN} - \beta V_{OUT} \qquad (1\text{-}29)$$

Rearranging terms puts the equation in recognizable form.

$$V_{OUT}\left(\frac{1}{A} + \beta\right) = V_{IN} \qquad (1\text{-}30)$$

This is the classical form of the feedback equation.

$$\left.\frac{V_{OUT}}{V_{IN}}\right| = \frac{1}{1+A\beta} \qquad (1\text{-}31)$$

The classic feedback equation reduces to the ideal feedback equation when $A\beta >> 1$.

$$\left.\frac{V_{OUT}}{V_{IN}}\right|_{A\beta>>1} = \frac{1}{\beta} \qquad (1\text{-}32)$$

Determining Stability

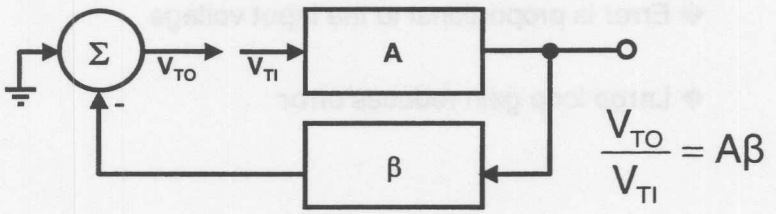
System Transfer Function

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta}$$

Conditions for Stability

$$1 + A\beta = 0$$

$$A\beta = -1 = \frac{|1|}{\angle 180°}$$



$$\frac{V_{TO}}{V_{TI}} = A\beta$$

Block Diagram For Computing The Loop Gain

1-29

The quantity Aβ is so important that it has been given a special name, loop gain. Consider the figure; when the voltage inputs are grounded (current inputs are opened) and the loop is broken the calculated gain is the loop gain, Aβ. Now, keep in mind that this is a mathematics of complex numbers which have magnitude and phase. When the loop gain approaches minus one, or to express it mathematically $1\angle 180°$, the classic feedback equation approaches infinity because $1/0 \Rightarrow \infty$. The circuit output heads for infinity as fast as it can using the equation of a straight line. If the output were not energy limited the circuit would explode the world, but it is energy limited by the power supplies so the world stays intact.

Active devices in electronic circuits exhibit non-linear behavior when their output approaches a power supply rail, and the non-linearity reduces the amplifier gain until the loop gain no longer equals $1\angle 180°$. Now the circuit can do two things: first it could become stable at the power supply limit, or second, it can reverse direction (because stored charge keeps the output voltage changing) and head for the negative power supply rail.

The first state where the circuit becomes stable at a power supply limit is named lockup; the circuit will remain in the locked up state until power is removed. The second state where the circuit bounces between power supply limits is named oscillatory. Remember, the loop gain, Aβ , is the sole factor that determines stability for a circuit or system. Inputs are grounded or disconnected when the loop gain is calculated, so they have no affect on stability.

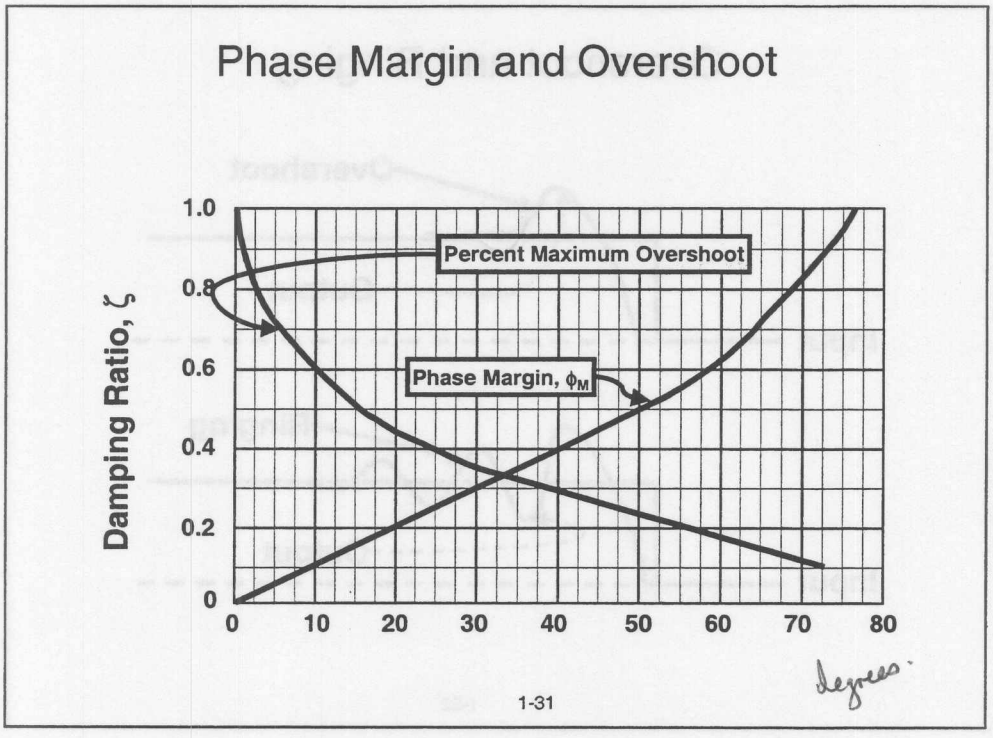
Feedback Circuit Accuracy

- Error Equation is $E = \frac{V_{IN}}{1 + A\beta}$
- Error is proportional to the input voltage
- Large loop gain reduces error

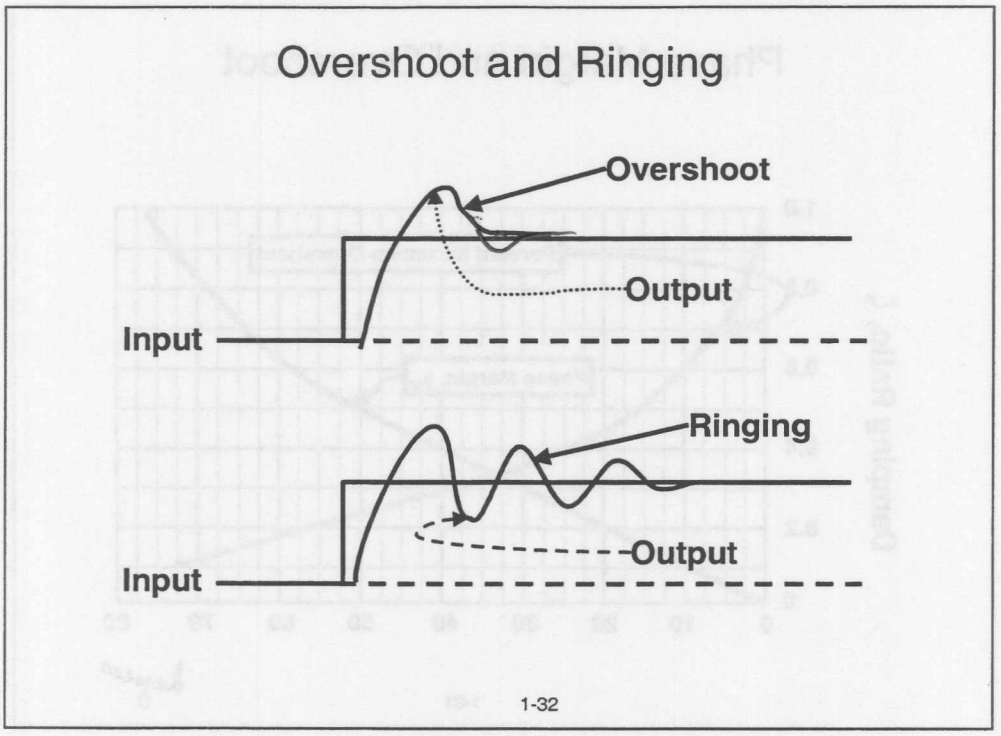
1-30

$$E = \frac{V_{IN}}{1 + A\beta} \qquad (1\text{-}33)$$

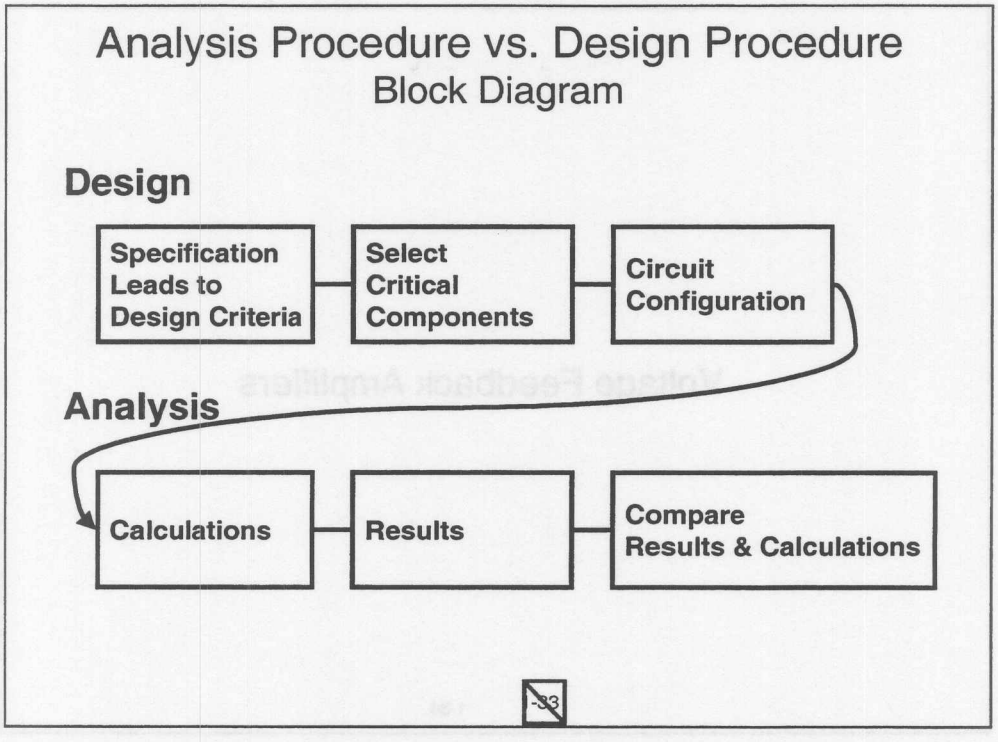
First, notice that the error is proportional to the input signal. This is the expected result because a bigger input signal results in a bigger output signal, and bigger output signals require more drive voltage. Second, the loop gain is inversely proportional to the error. As the loop gain increases the error decreases, thus large loop gains are attractive for minimizing errors. Large loop gains also decrease stability, thus there is always a tradeoff between error and stability.



The phase margin, and overshoot are plotted versus the damping ratio. Enter the graph at the calculated damping ratio, say 0.4, and read the overshoot at 25% and the phase margin at 42°. If a designer had a circuit specification of 5% overshoot, then the damping ratio must be 0.78 with a phase margin of 62°.

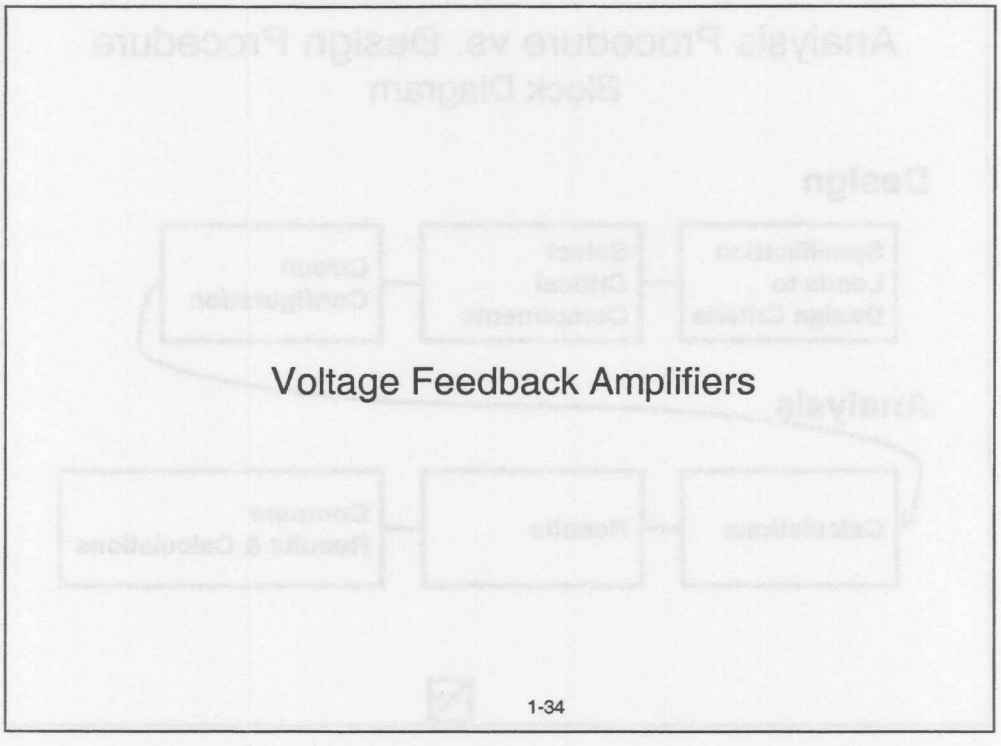


As the phase margin decreases the circuit tends towards instability. First, the circuit exhibits overshoot where the response overshoots the expected output value. Second, the circuit exhibits ringing where the response oscillates (decaying oscillation) above and below the expected output value. Third, oscillation which is ringing with no decay, results.

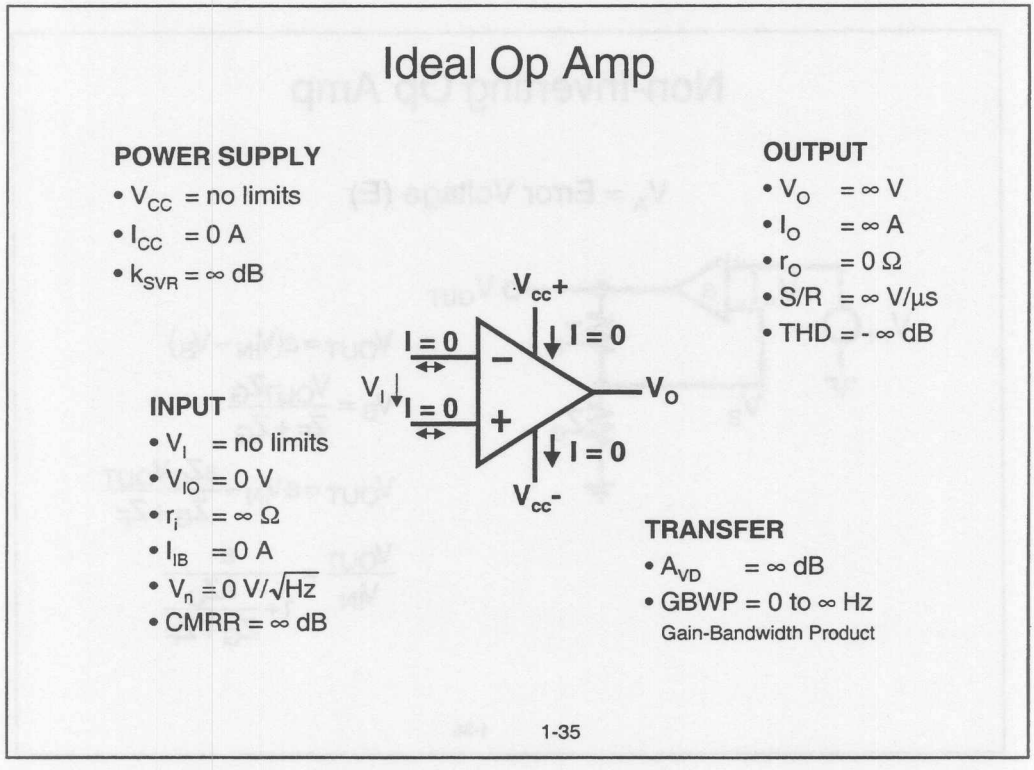


The design procedure starts with the specification. The designer creates an error budget based on the specifications. The most critical components (converters, DSP, etc.) are selected first, and their errors are subtracted from the error budget. The least critical components (op amps, interface, etc) are selected next, and their tolerance is selected to be within the error budget.

The circuit configuration has always been in mind when the components were selected, and now the circuit configuration is modified to accommodate the selected components. Analysis, which consists of calculations and results/specification verification, comes last.



There are two general classes of op amp feedback, and they are voltage feedback and current feedback. Voltage feedback was implemented first, and therefore is considered the standard. Current feedback followed voltage feedback, and it was developed to satisfy the demand for high frequency op amps.



Ideal Operational Amplifier

Before examining operational amplifiers, it may be helpful first to review the basic characteristics of an "ideal" op amp. And, it is convenient to group the characteristics into four categories: input -, output -, power supply -, and transfer characteristics. These are the four basic elements for evaluation in selecting a device for a given application as well.

The ideal op amp would have infinite input impedance (r_i) and no input bias currents (I_{IB}) causing no loading on the signal source. It would have infinite input differential voltage range (V_{ID}) as well as common-mode voltage range (CMRR) making no constraints on the properties of the input signal (V_I). There would be perfect matching of the input transistors leading to no dc input offset voltage (V_{IO}), and there would be no noise sources with no noise voltage (V_n) or current (I_n) generated by the op amp.

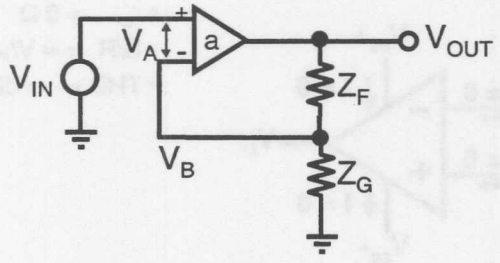
Moving to the output characteristics, the ideal op amp would be able to source or sink an infinite amount of current (I_O) with a rail to rail output swing with an infinite step response (no slew rate limitations (SR)) into any resistive, capacitive, or inductive load.

As to the characteristics of the power supply, there would be no minimum voltage requirement, nor a maximum voltage limit (V_{CC}). The device would consume no power, dissipate no power and it would work in split- and single-supply systems. For the transfer characteristics, the ideal op amp would have infinite open-loop gain (A_{VD}) and run at any frequency (GBWP) with no distortion (THD).

Of course, no op amp exhibits any of these characteristics, but an understanding of them will enable the designer to narrow his choices for further evaluation.

Non-Inverting Op Amp

V_A = Error Voltage (E)



$$V_{OUT} = a(V_{IN} - V_B)$$

$$V_B = \frac{V_{OUT} Z_G}{Z_F + Z_G}$$

$$V_{OUT} = aV_{IN} - \frac{aZ_G V_{OUT}}{Z_G + Z_F}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{a}{1 + \frac{aZ_G}{Z_G + Z_F}}$$

1-36

Equation 1-34 is the amplifier transfer equation.

$$V_{OUT} = a(V_{IN} - V_B) \qquad (1\text{-}34)$$

Equation 1-35 is the output equation.

$$\text{for } I_B = 0 \qquad V_B = \frac{V_{OUT} Z_G}{Z_F + Z_G} \qquad (1\text{-}35)$$

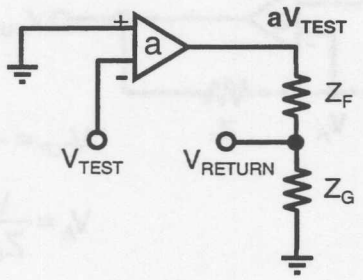
Combining equations 1-34 and 1-35 yields equation 1-36.

$$V_{OUT} = aV_{IN} - \frac{aZ_G V_{OUT}}{Z_G + Z_F} \qquad (1\text{-}36)$$

Rearranging terms in equation 1-36 yields equation 1-37 which describes the transfer function of the circuit.

$$\frac{V_{OUT}}{V_{IN}} = \frac{a}{1 + \frac{aZ_G}{Z_G + Z_F}} \qquad (1\text{-}37)$$

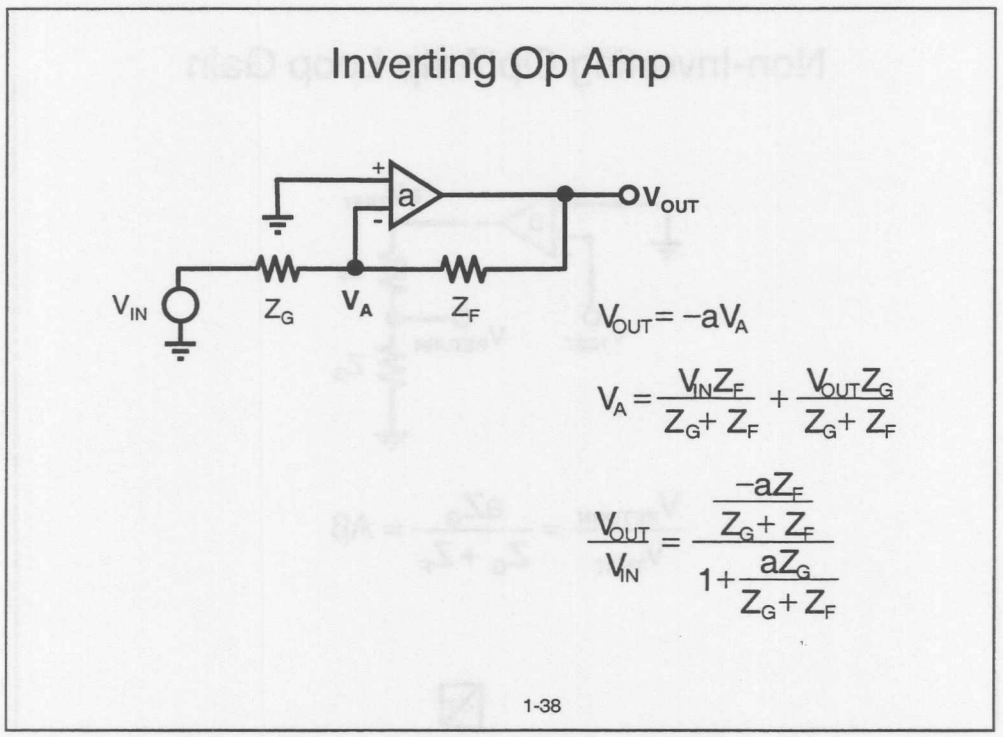
Non-Inverting Op Amp Loop Gain



$$\frac{V_{RETURN}}{V_{TEST}} = \frac{aZ_G}{Z_G + Z_F} = A\beta$$

-37

The non-inverting loop gain is calculated by breaking the loop and applying a test signal, V_{TEST}. First, voltage sources are grounded and current sources are open circuited. The return signal, V_{RETURN}, is calculated and then the loop gain is calculated as shown in the figure. The loop gain determines stability. The op amp inputs have no effect on stability because they are grounded or open circuited for the loop gain calculation.



The transfer equation for the inverting op amp circuit is given in equation 1-38.

$$V_{OUT} = -aV_A \quad (1\text{-}38)$$

The node voltage is described in equation 1-39, and equation 140 is obtained by combining equations 1-38 and 1-39.

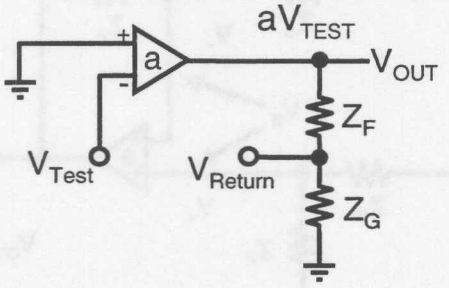
for $I_B = 0$

$$V_A = \frac{V_{IN}Z_F}{Z_G + Z_F} + \frac{V_{OUT}Z_G}{Z_G + Z_F} \quad (1\text{-}39)$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{-aZ_F}{Z_G + Z_F}}{1 + \frac{aZ_G}{Z_G + Z_F}} \quad (1\text{-}40)$$

Equation 1-40 is the transfer function of the inverting op amp.

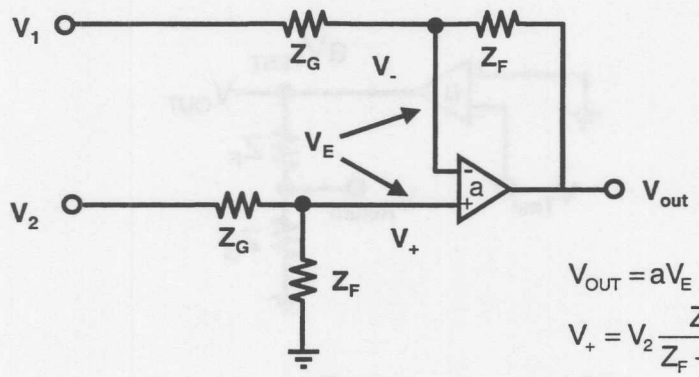
Inverting Op Amp Loop Gain



$$\frac{V_{RETURN}}{V_{TEST}} = \frac{aZ_G}{Z_G + Z_F} = A\beta$$

The non-inverting loop gain is calculated by breaking the loop and applying a test signal, V_{TEST}. First, voltage sources are grounded and current sources are open circuited. The return signal, V_{RETURN}, is calculated first, and then the loop gain is calculated as shown in the figure. The loop gain determines stability. The op amp inputs have no effect on stability because they are grounded or open circuited for the loop gain calculation.

The Differential Amplifier



$$V_{OUT} = aV_E$$

$$V_+ = V_2 \frac{Z_F}{Z_F + Z_G}$$

$$V_{OUT} = a\left(\frac{V_2 Z_F}{Z_F + Z_G} - \frac{V_1 Z_F}{Z_F + Z_G} - \frac{V_{OUT} Z_G}{Z_F + Z_G} \right)$$

$$\frac{V_{OUT}}{V_2 - V_1} = \frac{\frac{aZ_F}{Z_F + Z_G}}{1 + \frac{aZ_G}{Z_F + Z_G}}$$

1-40

The differential amplifier amplifies the difference signal applied to the input circuit, and it rejects the common mode portion of the input. This circuit configuration is often employed to strip dc or injected common mode noise off a signal.

Equation 1-41 is the circuit transfer equation:

$$V_{OUT} = aV_E = a(V_+ - V_-) \qquad (1\text{-}41)$$

The positive input voltage, V_+, is written in equation 1.4.9 with the aid of superposition and the voltage divider rule.

$$V_+ = V_2 \frac{Z_F}{Z_F + Z_G} \qquad (1\text{-}42)$$

The negative input voltage, V-, is written in equation 1-43 with the aid of superposition and the voltage divider rule:

$$V_- = V_1 \frac{Z_F}{Z_F + Z_G} - V_{OUT} \frac{Z_G}{Z_F + Z_G} \qquad (1\text{-}43)$$

Combining equations 1-14, 1-42 and 1-43 yields equation 1-44.

$$V_{OUT} = a\left[\frac{V_2 Z_F}{Z_F + Z_G} - \frac{V_1 Z_F}{Z_F + Z_G} - \frac{V_{OUT} Z_G}{Z_F + Z_G} \right] \qquad (1\text{-}44)$$

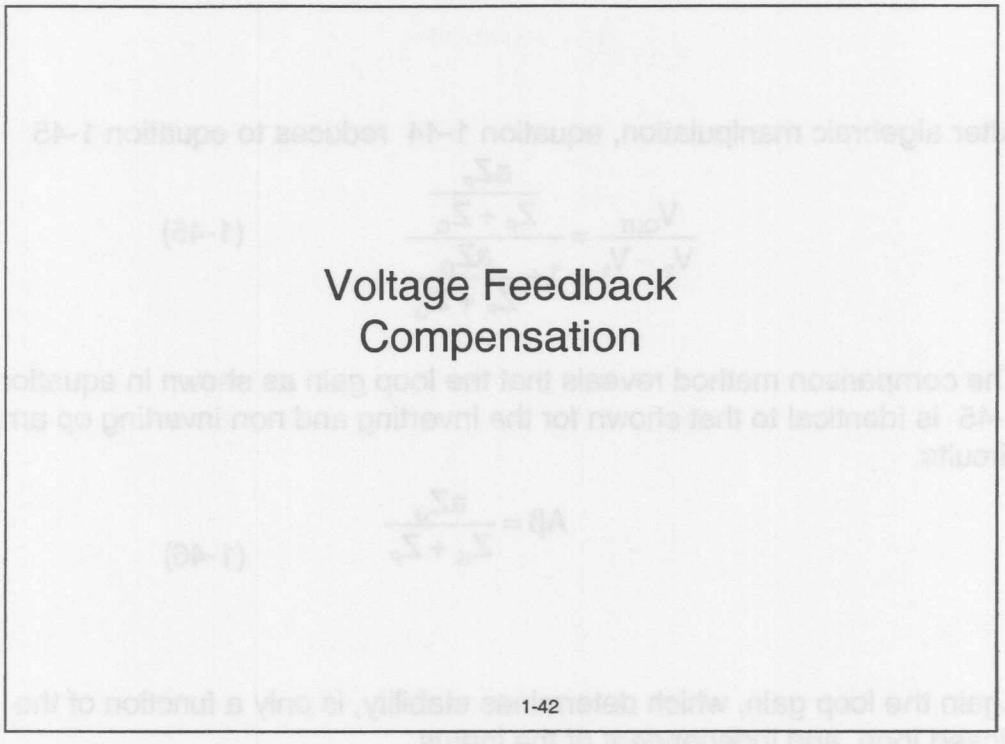
After algebraic manipulation, equation 1-44 reduces to equation 1-45

$$\frac{V_{OUT}}{V_2 - V_1} = \frac{\dfrac{aZ_F}{Z_F + Z_G}}{1 + \dfrac{aZ_G}{Z_F + Z_G}} \qquad (1\text{-}45)$$

The comparison method reveals that the loop gain as shown in equation 1-45 is identical to that shown for the inverting and non inverting op amp circuits.

$$A\beta = \frac{aZ_G}{Z_G + Z_F} \qquad (1\text{-}46)$$

Again the loop gain, which determines stability, is only a function of the closed loop, and independent of the inputs.



Voltage feedback amplifiers (VFA) have been with us for about 60 years, and they have been a problem for circuit designers since the first day. You see, the feedback that makes them versatile and accurate also has a tendency to make them unstable. The operational amplifier (op amp) circuit configuration uses a high gain amplifier whose parameters are determined by external feedback components. The amplifier gain is so high that the slightest input signal would saturate the amplifier output without these external feedback components. The op amp is in common usage, so this configuration is examined in detail, but the results are applicable to many other voltage feedback circuits. Current feedback amplifiers (CFA) are similar to VFAs, but the differences are important enough to warrant CFAs being handled in a separate application note.

Feedback circuits exhibit poor phase response, overshoot, and ringing long before oscillation occurs, and these effects are considered undesirable by circuit designers. Relative stability is defined in terms of performance. By definition, when designers decide what tradeoffs are acceptable they determine what the relative stability of the circuit is. A relative stability measurement is the damping ratio, ζ. The damping ratio is related to phase margin, hence phase margin is another measure of relative stability.

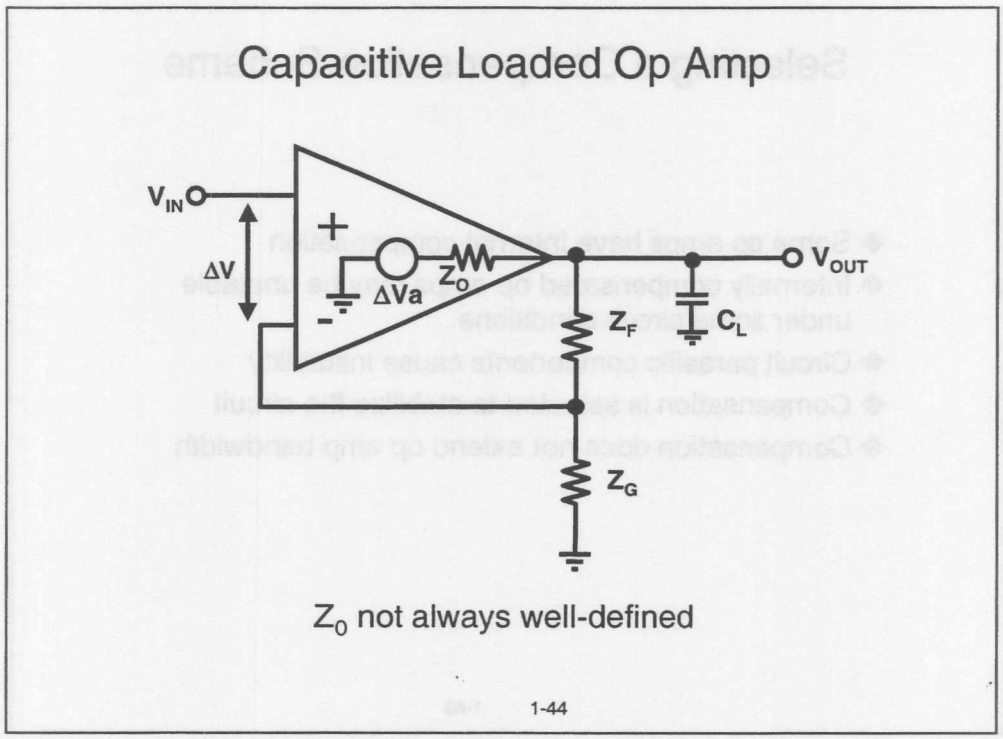
Selecting a Compensation Scheme

- Some op amps have internal compensation
- Internally compensated op amps may be unstable under some circuit conditions
- Circuit parasitic components cause instability
- Compensation is selected to stabilize the circuit
- Compensation does not extend op amp bandwidth

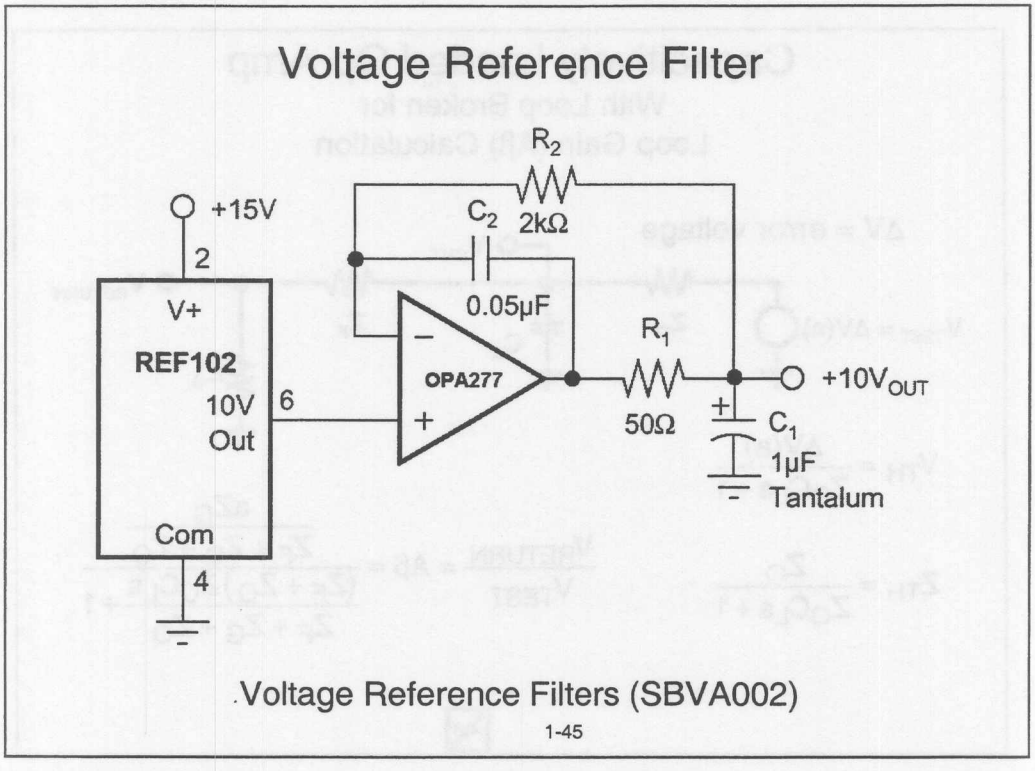
1-43

Non-internally compensated or "externally" compensated op amps are unstable without the addition of external stabilizing components. This situation is a disadvantage in many cases because they require additional components, but the lack of internal compensation enables the top drawer circuit designer to squeeze the last drop of performance from the op amp. You have two options: op amps internally compensated by the IC manufacturer, or externally compensated by you. Compensation, except that done by the op amp manufacturer, must be done external to the IC. Surprisingly enough, internally compensated op amps require external compensation for demanding applications.

Compensation is achieved by adding external components that modify the circuit transfer function so that it becomes unconditionally stable. There are several different methods of compensating an op amp, and as you might suspect, there are pros and cons associated with each method of compensation. Teaching you how to compensate and how to evaluate the results of compensation is the intent of this seminar. After the op amp circuit is compensated, it must be analyzed to determine the effects of compensation. The modifications that compensation have on the closed loop transfer function often determine which compensation scheme is most profitably employed.



Capacitive loading causes potential instabilities, thus an op amp loaded with an output capacitor is a circuit configuration that must be analyzed. This circuit is called dominant pole compensation because if the pole formed by the op amp output impedance and the loading capacitor is located close to the zero frequency axis it becomes dominant.

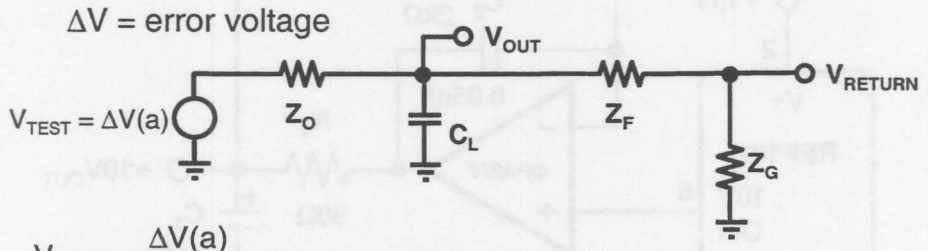


This is a practical example of an amplifier driving a capacitive load. Connecting a large value capacitor on the output of an op amp will form another pole in the Bode plot. This extra pole, R_1 with C_1, might cause the amplifier to break into oscillations. The addition of R_2 and C_2 will stabilize the circuit.

Additional information about this circuit can be found in application note SBVA002.

Capacitively Loaded Op Amp

With Loop Broken for
Loop Gain (Aβ) Calculation



$$V_{TH} = \frac{\Delta V(a)}{Z_O C_L s + 1}$$

$$Z_{TH} = \frac{Z_O}{Z_O C_L s + 1}$$

$$\frac{V_{RETURN}}{V_{TEST}} = A\beta = \frac{\dfrac{aZ_G}{Z_F + Z_G + Z_O}}{\dfrac{(Z_F + Z_O)Z_O C_L s}{Z_F + Z_G + Z_O} + 1}$$

The analysis starts by looking into the capacitor and taking the Thevenin equivalent circuit.

$$V_{TH} = \frac{\Delta V(a)}{Z_O C_L s + 1} \quad (1\text{-}47) \qquad Z_{TH} = \frac{Z_O}{Z_O C_L s + 1} \quad (1\text{-}48)$$

Then the loop gain equation is written.

$$\frac{V_{RETURN}}{V_{TEST}} = A\beta = \frac{\dfrac{aZ_G}{Z_F + Z_G + Z_O}}{\dfrac{(Z_F + Z_G)Z_O C_L s}{Z_F + Z_G + Z_O} + 1} \quad (1\text{-}49)$$

When the assumption is made that $(Z_F + Z_G) >> Z_O$ equation 1-49 reduces to equation 1-50.

$$A\beta = \frac{aZ_G}{Z_F + Z_G}\left(\frac{1}{Z_O C_L s + 1}\right) \quad (1\text{-}50)$$

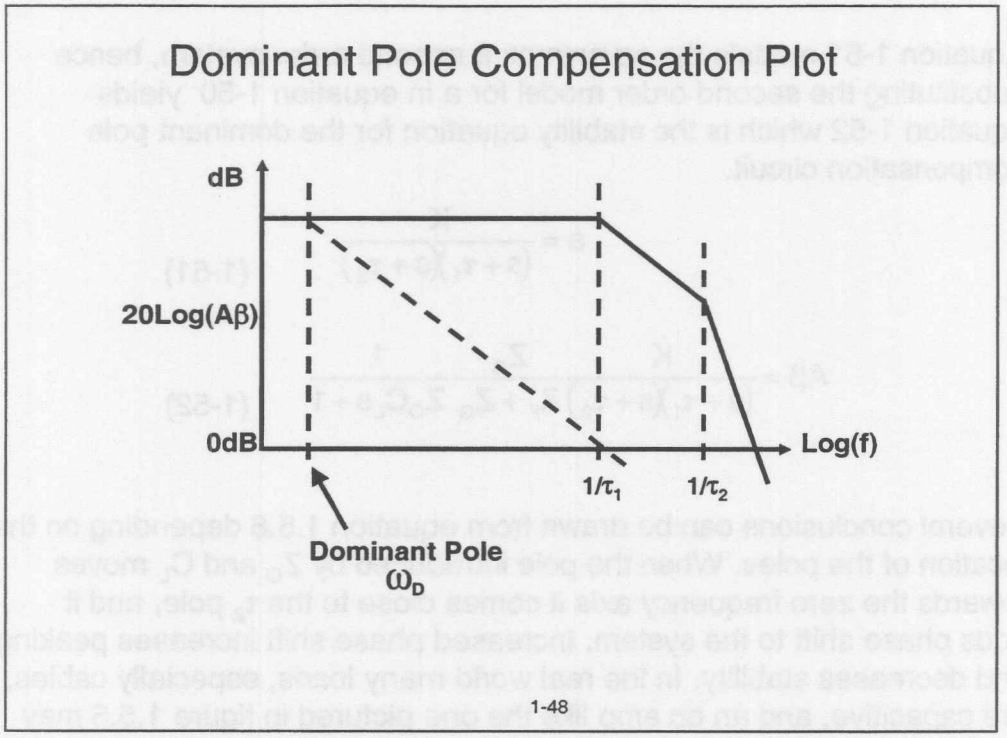
.

Equation 1-51 models the op amp as a second order system, hence substituting the second order model for a in equation 1-50 yields equation 1-52 which is the stability equation for the dominant pole compensation circuit.

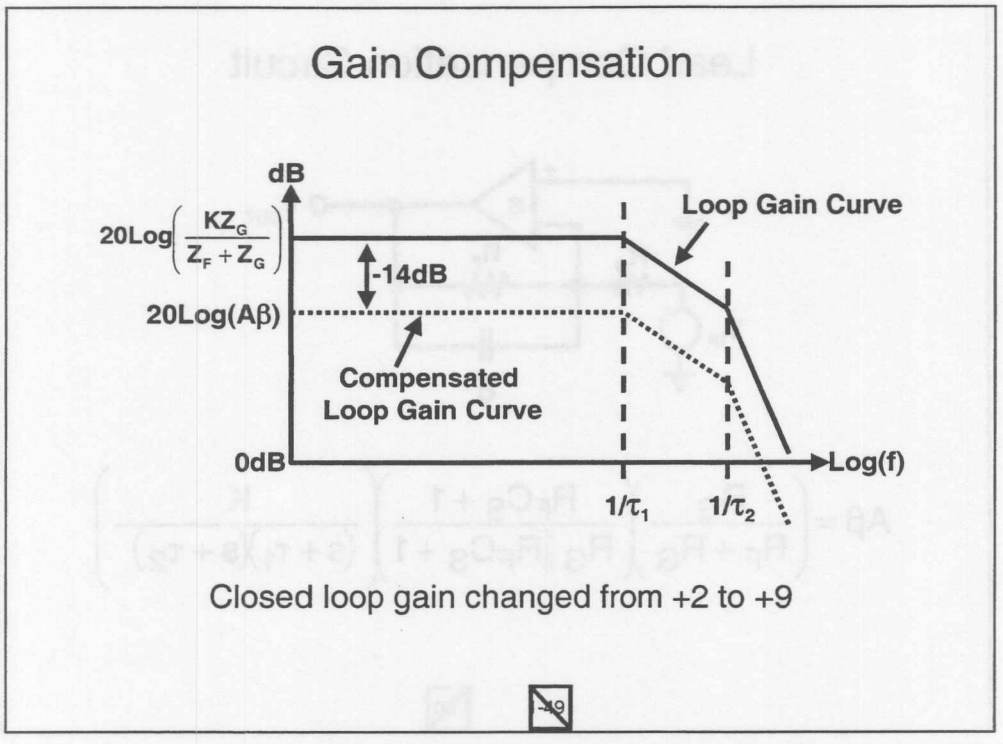
$$a = \frac{K}{(s+\tau_1)(s+\tau_2)} \qquad (1\text{-}51)$$

$$A\beta = \frac{K}{(s+\tau_1)(s+\tau_2)} \frac{Z_G}{Z_F + Z_G} \frac{1}{Z_O C_L s + 1} \qquad (1\text{-}52)$$

Several conclusions can be drawn from equation 1.5.6 depending on the location of the poles. When the pole introduced by Z_O and C_L moves towards the zero frequency axis it comes close to the τ_2 pole, and it adds phase shift to the system. Increased phase shift increases peaking and decreases stability. In the real world many loads, especially cables, are capacitive, and an op amp like the one pictured in figure 1.5.3 may ring while driving a capacitive load. The load capacitance causes peaking and instability in internally compensated op amps when the op amps do not have enough phase margin to allow for the phase shift introduced by the load.



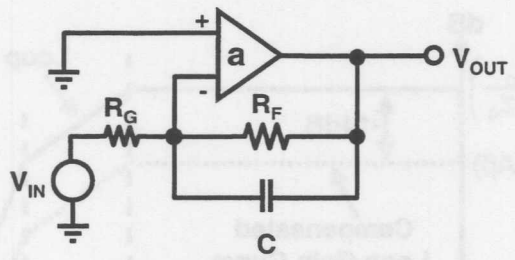
Prior to compensation, the Bode plot of an uncompensated op amp looks like that shown in the figure. Notice that the break points are located close together thus accumulating about 180° of phase shift before the 0dB crossover point; the op amp is not usable and probably unstable. Dominant pole compensation is often used to stabilize these op amps. If a dominant pole, in this case ω_D, is properly placed it rolls off the gain so that τ_1 introduces 45° phase at the 0dB crossover point. After the dominant pole is introduced the op amp is stable with 45° phase margin, but the op amp gain is drastically reduced for frequencies above ω_D. This procedure works well for internally compensated op amps, but is seldom used for externally compensated op amps because other compensation techniques are readily available.



The original loop gain curve for a closed loop gain of one is shown in the figure and it is or comes very close to being unstable. If the closed loop non-inverting gain is changed to 9, then K changes from K/2 to K/10. The loop gain intercept on the Bode plot moves down 14dB, and the circuit is stabilized.

Gain compensation works for inverting or non-inverting op amp circuits because the loop gain equation contains the closed loop gain parameters in both cases. When the closed loop gain is increased, the accuracy and the bandwidth decrease. As long as the application can stand the higher gain, gain compensation is the best type of compensation to use. Uncompensated versions of internally compensated op amps are offered for sale as internally compensated op amps with minimum gain restrictions. As long as the closed loop gain exceeds the specified gain this is economical and a safe mode of operation.

Lead Compensation Circuit



$$A\beta = \left(\frac{R_G}{R_F + R_G}\right)\left(\frac{R_F C_S + 1}{R_G \| R_F C_S + 1}\right)\left(\frac{K}{(s+\tau_1)(s+\tau_2)}\right)$$

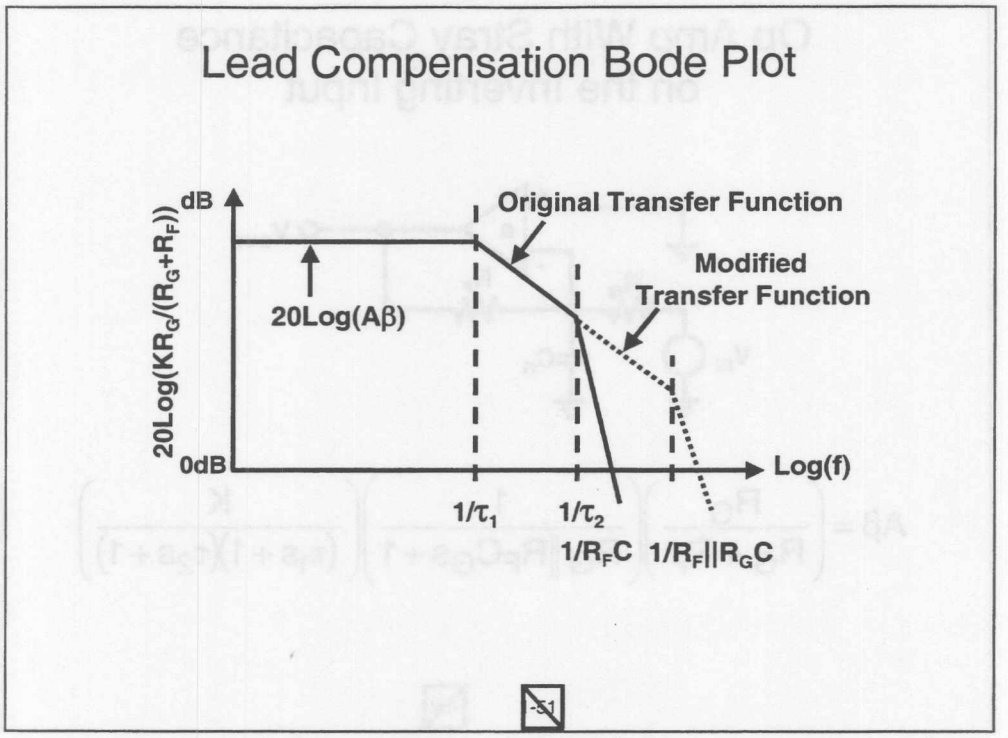
1-50

Sometimes lead compensation is forced on the circuit designer because of the parasitic capacitance associated with packaging and wiring op amps. Figure 1-50 shows the circuit for lead compensation; notice the capacitor in parallel with R_F. That capacitor is often made by parasitic wiring and the ground plane, and high frequency circuit designers go to great lengths to minimize or eliminate it. One man's pig is another man's pearl, because adding the parallel capacitor is a good way to stabilize the op amp and reduce noise.

The loop equation for the lead compensation circuit is given in equation 1-53.

$$A\beta = \left(\frac{R_G}{R_G + R_F}\right)\left(\frac{R_F C s + 1}{R_G \| R_F C s + 1}\right)\left(\frac{K}{(s+\tau_1)(s+\tau_2)}\right) \quad (1\text{-}53)$$

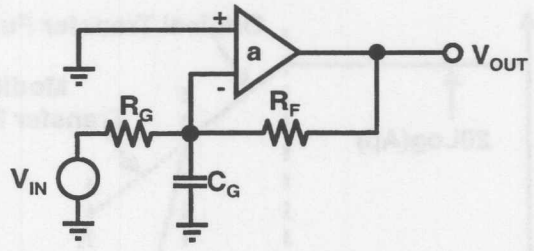
The compensation capacitor introduces a pole and zero into the loop equation. The zero always occurs before the pole because $R_F > R_F \| R_G$. When the zero is properly placed it cancels out the τ_2 pole along with its associated phase shift.



The original transfer function is shown in figure 1-51 drawn in solid lines. When the R_FC zero is placed at $\omega = 1/\tau_2$, it cancels out the τ_2 pole causing the bode plot to continue on a slope of -20dB/decade. When the frequency gets to $\omega = 1/(R_F||RG)C$, this pole changes the slope to -40dB/decade. Properly placed, the capacitor aids stability.

The feedback capacitor causes the op amp gain to roll off, thus the closed loop bandwidth is decreased. Adding this capacitor stabilizes the circuit while reducing the closed loop bandwidth.

Op Amp With Stray Capacitance on the Inverting Input



$$A\beta = \left(\frac{R_G}{R_G + R_F}\right)\left(\frac{1}{R_G \| R_F C_G s + 1}\right)\left(\frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)}\right)$$

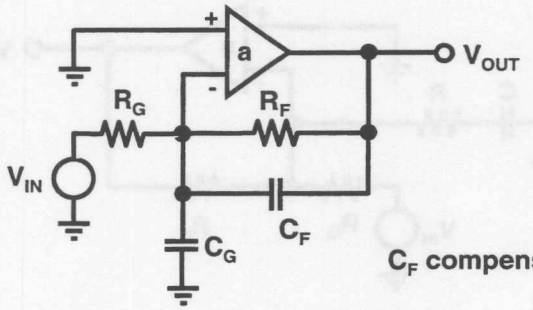
1-52

Stray capacitance on op amp inputs is a problem that circuit designers are always trying to get away from because causes peaking. The circuit shown in figure 1-52 has some stray capacitance, C_G, connected from the inverting input to ground. Equation 1-54 is the loop gain equation for the circuit with input capacitance.

$$A\beta = \left(\frac{R_G}{R_G + R_F}\right)\left(\frac{1}{R_G \| R_F C_G s + 1}\right)\left(\frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)}\right) \quad (1\text{-}54)$$

Op amps having high input value and feedback resistors are subject to instability caused by stray capacitance on the inverting input. When the $1/(R_F||R_GC_G)$ pole moves close to τ_2 the stage is set for instability. Reasonable component values for a CMOS op amp are R_F = 1MΩ, R_G = 1MΩ, and C_G = 10pF. The resulting pole occurs at 318kHz, and this frequency is lower than the breakpoint of τ_2 for many op amps. There is 90° phase shift resulting from τ_1, the $1/(R_F||R_GC)$ pole adds 45° phase shift at 318kHz, and τ_2 starts adds another 45° phase shift at about 600kHz. This circuit is unstable because of the stray input capacitance.

Compensated Attenuator Circuit



$$A\beta = \left(\frac{\frac{R_G}{R_G C_G s + 1}}{\frac{R_G}{R_G C_G s + 1} + \frac{R_F}{R_F C_F s + 1}} \right) a$$

-53

The circuit is compensated by adding a feedback capacitor as shown in figure 1-53.

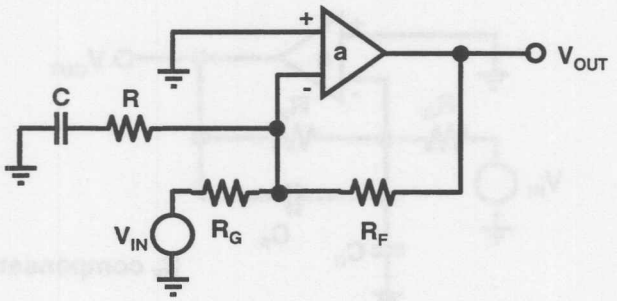
$$A\beta = \left(\frac{\frac{R_G}{R_G C_G s + 1}}{\frac{R_G}{R_G C_G s + 1} + \frac{R_F}{R_F C_F s + 1}} \right) \left(\frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)} \right) \quad (1\text{-}55)$$

If $R_G C_G = R_F C_F$ equation 1-55 reduces to equation 1-56.

$$A\beta = \left(\frac{R_G}{R_G + R_F} \right) \left(\frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)} \right) \quad (1\text{-}56)$$

This compensation cancels the effect of C_G, but it does not cancel the effects of the op amp poles τ_1 and τ_2.

Lead-Lag Compensated Op Amp

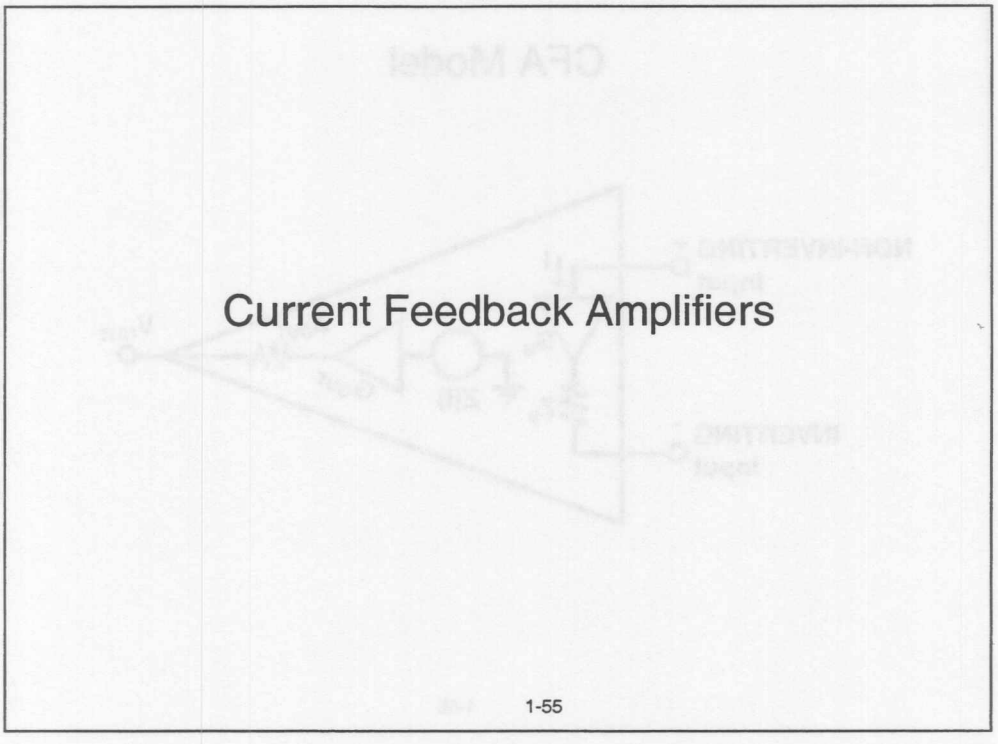


$$A\beta = \left(\frac{K}{(\tau_1 s+1)(\tau_2 s+1)}\right)\left(\frac{R_G}{R_F+R_G}\right)\left(\frac{RCs+1}{\frac{(RR_G+RR_F+R_GR_F)}{R_G+R_F}Cs+1}\right)$$

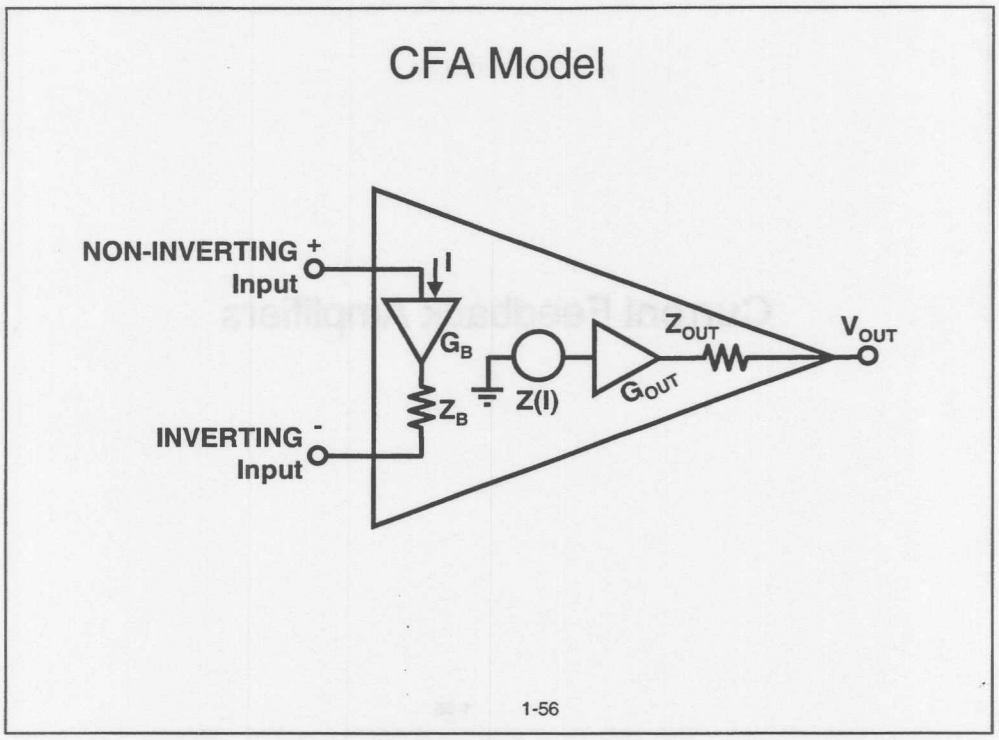
1-54

Lead-lag compensation stabilizes the circuit without sacrificing the closed loop gain performance. This type of compensation leads to excellent high frequency performance. The circuit schematic is shown in figure 1-54 and the loop gain is given in equation 1-57.

$$A\beta = \frac{K}{(\tau_1 s+1)(\tau_2 s+1)}\frac{R_G}{R_G+R_F}\frac{RCs+1}{\frac{(RR_G+RR_F+R_GR_F)}{(R_G+R_F)}Cs+1} \qquad (1\text{-}57)$$



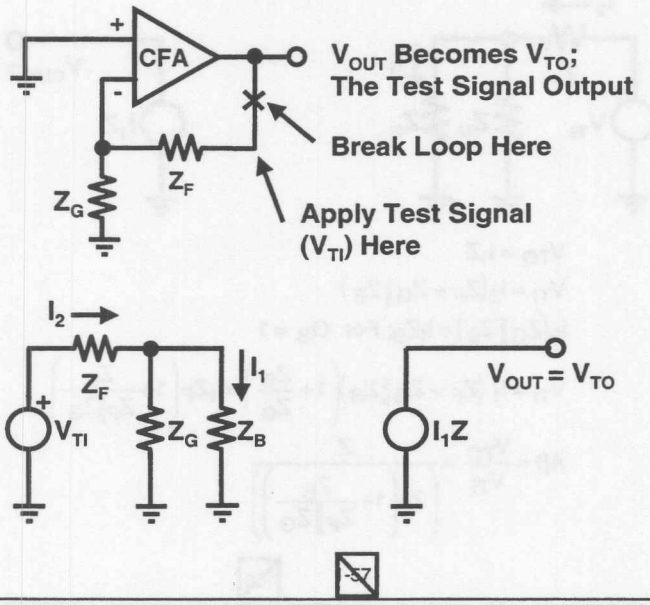
Current feedback amplifiers (CFA) have sacrificed the DC precision of voltage feedback amplifiers (VFB) for speed. This tradeoff results in higher bandwidth, faster slew rate, and a bandwidth that is relatively independent of closed loop gain. Although CFAs do not have the precision of their VFB counterparts, they can be DC coupled in video applications without sacrificing much dynamic range. CFAs have eliminated the AC coupling requirement in high frequency amplifiers because they operate in the GHz range while DC coupled. CFAs have much faster slew rates than VFAs, so they have faster rise/fall times and less intermodulation distortion.



The non-inverting input of a CFA connects to the input of a buffer, so it has a very high impedance similar to a bipolar transistor VFA input. The inverting input connects to the buffer's output, so the inverting input impedance is very low. Z_B models the input buffer's output impedance which is usually less than 50Ω. The buffer gain, G_B, is as close to one as IC design methods can achieve, so it is neglected in the calculations.

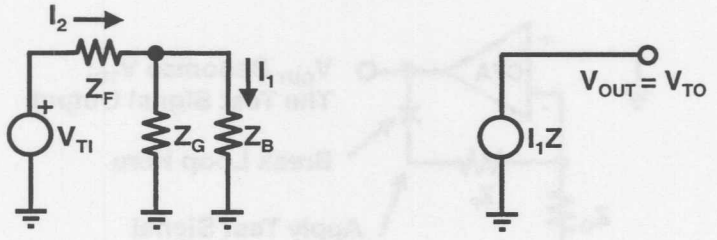
The output buffer is used to give the amplifier a low output impedance. Again the gain, G_{OUT}, is very close to one, so it is neglected in this analysis. The impedance of the output buffer can be ignored except when driving very low impedance or capacitive loads. The input buffer's output impedance can't be ignored because it affects stability at high frequencies. The current-controlled current source, Z, is a transimpedance. The transimpedance in a CFA serves the same function as the gain in a VFA. Usually the transimpedance is very high, in the MΩ range, so the CFA gains accuracy in the same manner that the VFA does.

Stability Analysis Circuit



Stability is independent of the input, and stability depends solely on the loop gain, Aβ. The stability equation is developed by breaking the loop at point "X", inserting a test signal, V_{TI}, and calculating the return signal V_{TO}. The input buffer gain, the output buffer gain and the output buffer output impedance have been left out of the circuit to simplify calculations. This approximation is valid for almost all applications.

Stability Analysis



$$V_{TO} = I_1 Z$$

$$V_{TI} = I_2\left(Z_F + Z_G \| Z_B\right)$$

$$I_2\left(Z_G \| Z_B\right) = I_1 Z_B;\ \text{For}\ G_B = 1$$

$$V_{TI} = I_1\left(Z_F + Z_G \| Z_B\right)\left(1 + \frac{Z_B}{Z_G}\right) = I_1 Z_F\left(1 + \frac{Z_B}{Z_F \| Z_G}\right)$$

$$A\beta = \frac{V_{TO}}{V_{TI}} = \frac{Z}{\left(Z_F\left(1 + \frac{Z_B}{Z_F \| Z_G}\right)\right)}$$

1-58

The transfer equation is given in equation 1-58, and the Kirchoff"s law is used to write equations 1-59 and 1-60.

$$V_{TO} = I_1 Z \qquad (1\text{-}58)$$

$$V_{TI} = I_2\left(Z_F + Z_G \| Z_B\right) \qquad (1\text{-}59)$$

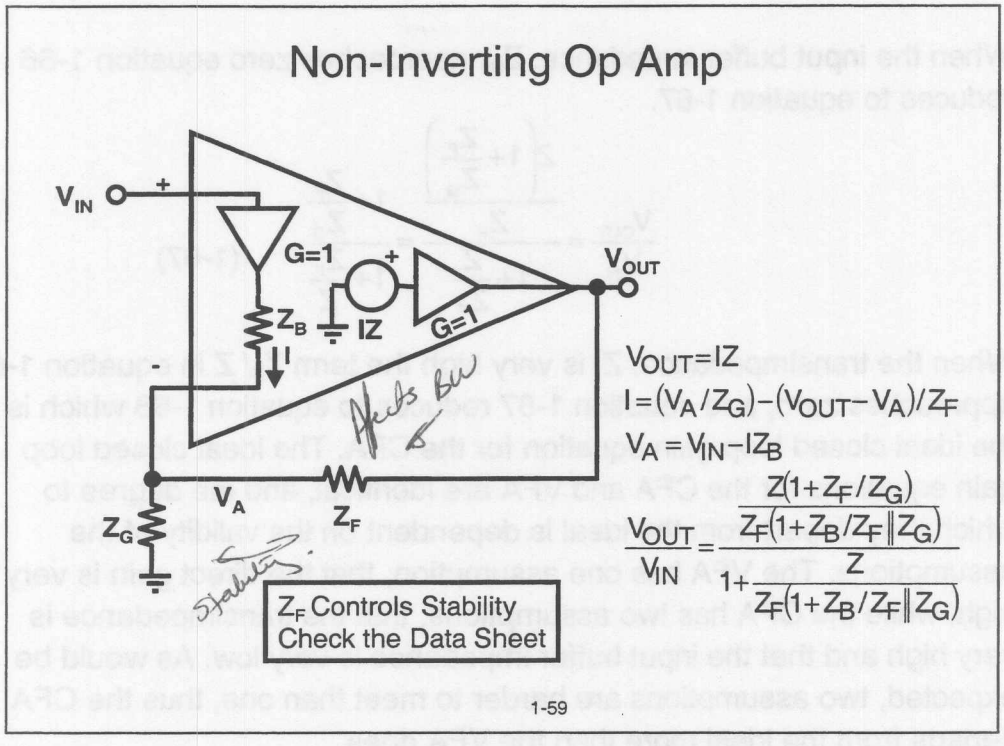
$$I_2\left(Z_G \| Z_B\right) = I_1 Z_B \qquad (1\text{-}60)$$

Equations 1-59 and 1-60 are combined to yield equation 1-61.

$$V_{TI} = I_1\left(Z_F + Z_G \| Z_B\right)\left(1 + \frac{Z_B}{Z_G}\right) = I_1 Z_F\left(1 + \frac{Z_B}{Z_F \| Z_G}\right) \qquad (1\text{-}61)$$

Dividing equation 1-58 by equation 1-61 yields equation 1-62 which is the open loop transfer equation which is commonly known as the loop gain.

$$A\beta = \frac{V_{TO}}{V_{TI}} = \frac{Z}{\left(Z_F\left(1 + \frac{Z_B}{Z_F \| Z_G}\right)\right)} \qquad (1\text{-}62)$$



Equation 1-63 is the transfer equation, equation 1-64 is the current equation at the inverting node, and equation 1-65 is the input loop equation. These equations are combined to yield equation 1-66 which is the closed loop gain equation.

$$V_{OUT} = IZ \qquad (1\text{-}63)$$

$$I = \left(\frac{V_A}{Z_G}\right) - \left(\frac{V_{OUT} - V_A}{Z_F}\right) \qquad (1\text{-}64)$$

$$V_A = V_{IN} - IZ_B \qquad (1\text{-}65)$$

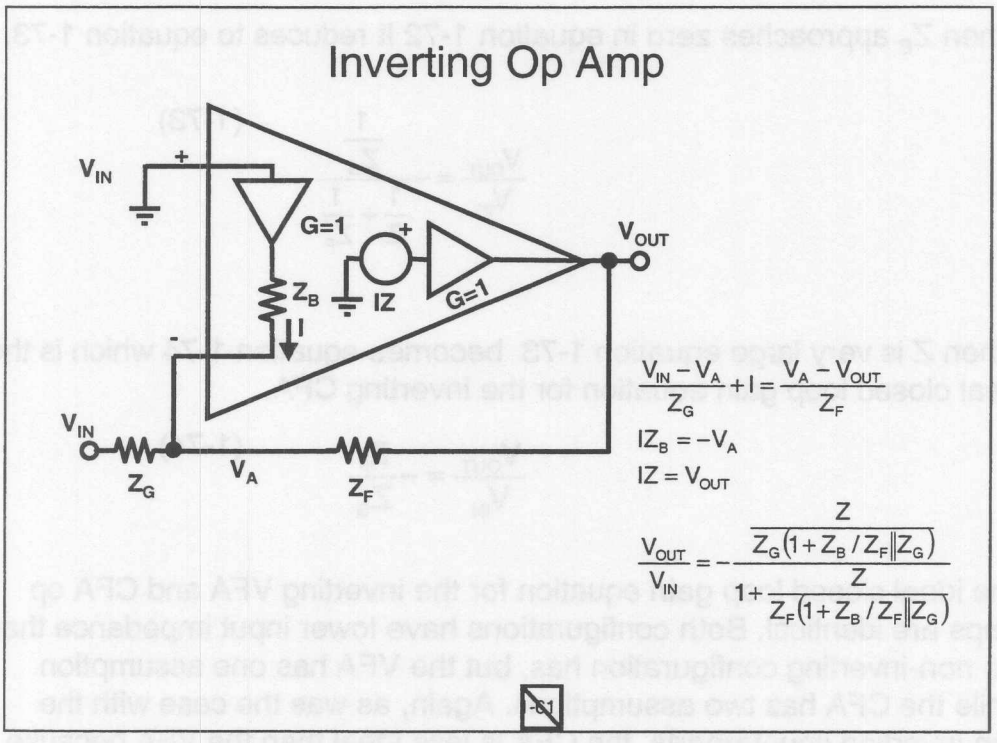
$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{Z\left(1+\frac{Z_F}{Z_G}\right)}{Z_F\left(1+\frac{Z_B}{Z_F \| Z_G}\right)}}{1+\frac{Z}{Z_F\left(1+\frac{Z_B}{Z_F \| Z_G}\right)}} \qquad (1\text{-}66)$$

When the input buffer impedance, Z_B, approaches zero equation 1-66 reduces to equation 1-67.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{Z\left(1+\frac{Z_F}{Z_G}\right)}{Z_F}}{1+\frac{Z}{Z_F}} = \frac{1+\frac{Z_F}{Z_G}}{1+\frac{Z_F}{Z}} \qquad (1\text{-}67)$$

When the transimpedance, Z, is very high the term Z_F/Z in equation 1-67 approaches zero, and equation 1-67 reduces to equation 1-68 which is the ideal closed loop gain equation for the CFA. The ideal closed loop gain equations for the CFA and VFA are identical, and the degree to which they depart from the ideal is dependent on the validity of the assumptions. The VFA has one assumption, that the direct gain is very high, while the CFA has two assumptions, that the transimpedance is very high and that the input buffer impedance is very low. As would be expected, two assumptions are harder to meet than one, thus the CFA departs from the ideal more than the VFA does.

$$\frac{V_{OUT}}{V_{IN}} = 1+\frac{Z_F}{Z_G} \qquad (1\text{-}68)$$



The inverting CFA configuration is seldom used because the input impedance is very low ($Z_B||Z_F + Z_G$). When Z_G is selected as high resistance to swamp out the effects of Z_B, Z_F must also be high. High values for Z_F result in poor bandwidth performance. If Z_G is selected as a low value, Z_B, which is frequency sensitive, causes the gain to increase as frequency increases. These limitations restrict the applications for the inverting CFA.

The current equation for the input node is written as equation 1-69. Equation 1-70 defines the dummy variable, V_A, and equation 1-71 is the transfer equation for the CFA. These equations are combined and simplified leading to equation 1-72 which is the closed loop gain equation for the inverting CFA.

$$1+\frac{V_{IN}-V_A}{Z_G}=\frac{V_A-V_{OUT}}{Z_F} \quad (1\text{-}69)$$

$$IZ_B=-V_A \quad (1\text{-}70) \qquad IZ=V_{OUT} \quad (1\text{-}71)$$

$$\frac{V_{OUT}}{V_{IN}}=-\frac{\frac{Z}{Z_G\left(1+\frac{Z_B}{Z_F\|Z_G}\right)}}{1+\frac{Z}{Z_F\left(1+\frac{Z_B}{Z_F\|Z_G}\right)}} \quad (1\text{-}72)$$

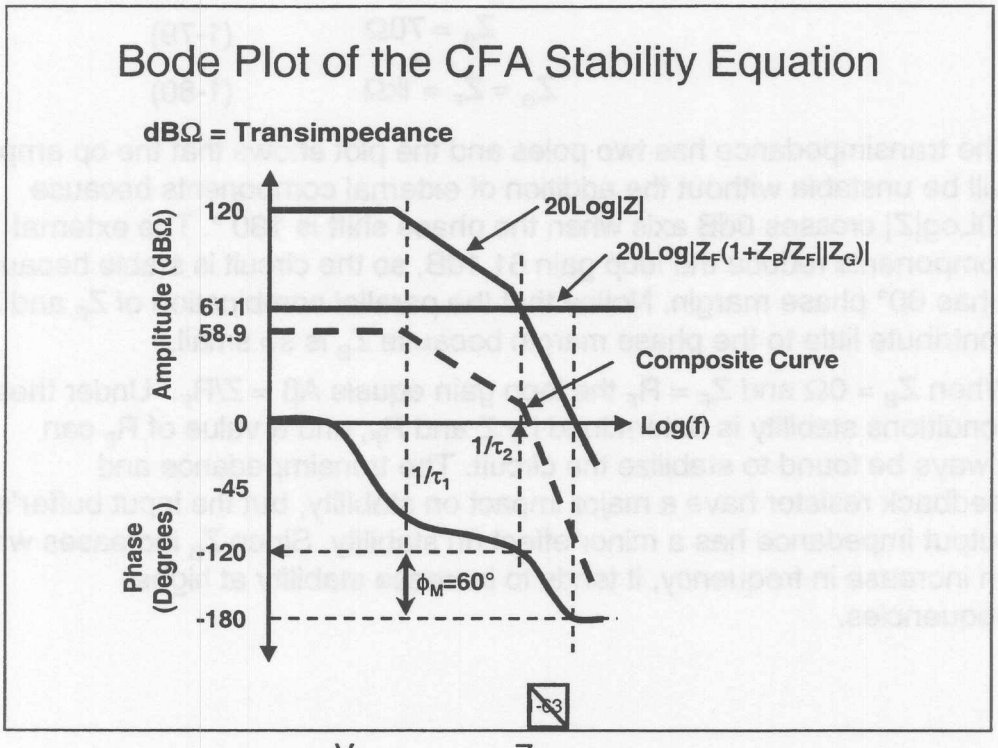
When Z_B approaches zero in equation 1-72 it reduces to equation 1-73.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{\frac{1}{Z_G}}{\frac{1}{Z} + \frac{1}{Z_F}} \qquad (1\text{-}73)$$

When Z is very large equation 1-73 becomes equation 1-74 which is the ideal closed loop gain equation for the inverting CFA.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_F}{Z_G} \qquad (1\text{-}74)$$

The ideal closed loop gain equation for the inverting VFA and CFA op amps are identical. Both configurations have lower input impedance than the non-inverting configuration has, but the VFA has one assumption while the CFA has two assumptions. Again, as was the case with the non-inverting counterparts, the CFA is less ideal than the VFA because of the two assumptions.



$$A\beta = \frac{V_{TO}}{V_{TI}} = \frac{Z}{\left(Z_F\left(1+\frac{Z_B}{Z_F \| Z_G}\right)\right)} \quad (1\text{-}75)$$

The two op amp parameters affecting stability are the transimpedance, Z, and the input buffer's output impedance, Z_B. The external components affecting stability are Z_G and Z_F. The external impedances are controlled by the designer, although stray capacitance which is a part of the external impedance sometimes seems to be uncontrollable. Z and Z_B are CFA op amp parameters, and they can't be controlled by the circuit designer, so he has to live with them. We take the log of equation 1-75 prior to plotting the logs which are equations 1-76 and 1-77.

$$20LOG|A\beta| = 20Log|Z| - 20Log\left|Z_F\left(1+\frac{Z_B}{Z_F \| Z_B}\right)\right| \quad (1\text{-}76)$$

$$\phi = Tangent^{-1}(A\beta) \quad (1\text{-}77)$$

The log plot, called a Bode plot, is named after H. W. Bode who first developed it in the forties. It enables the designer to add and subtract components of the stability equation graphically.

The Bode plot of the CFA assumes typical values for the parameters:

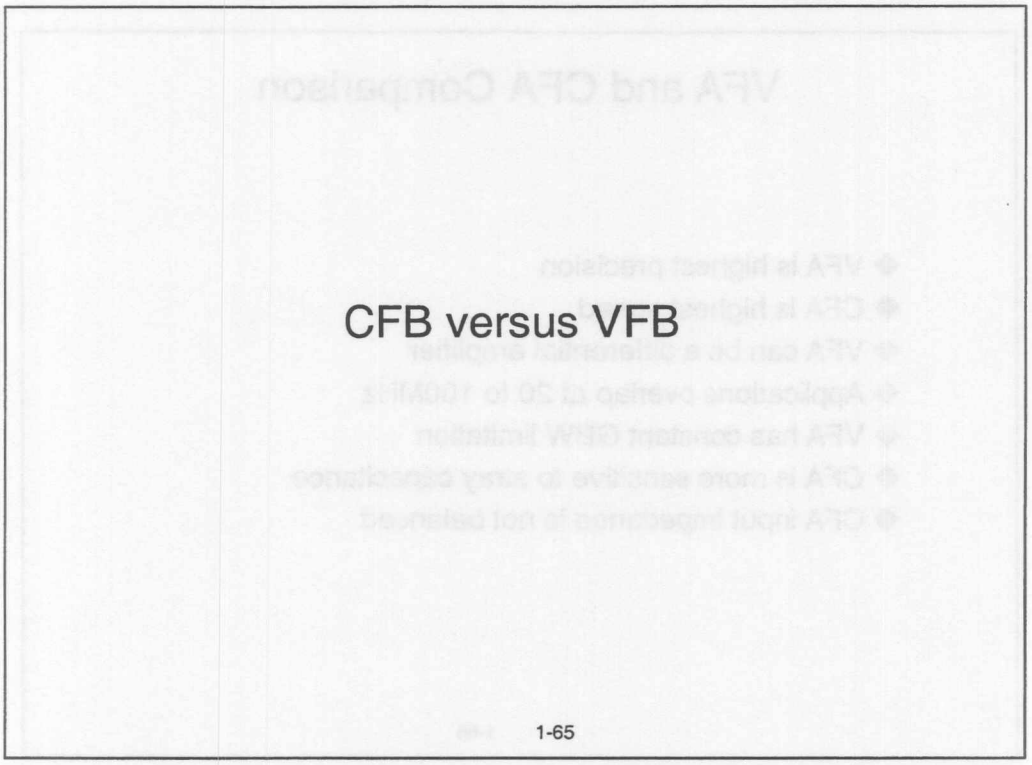
$$Z = \frac{1M\Omega}{(1+\tau_1 s)(1+\tau_2 s)} \quad (1\text{-}78)$$

$$Z_B = 70\Omega \qquad (1\text{-}79)$$

$$Z_G = Z_F = 1k\Omega \qquad (1\text{-}80)$$

The transimpedance has two poles and the plot shows that the op amp will be unstable without the addition of external components because 20Log|Z| crosses 0dB axis when the phase shift is 180 °. The external components reduce the loop gain 61.1dB, so the circuit is stable because it has 60° phase margin. Notice that the parallel combination of Z_F and Z_G contribute little to the phase margin because Z_B is so small.

When $Z_B = 0\Omega$ and $Z_F = R_F$ the loop gain equals $A\beta = Z/R_F$. Under these conditions stability is determined by Z and R_F, and a value of R_F can always be found to stabilize the circuit. The transimpedance and feedback resistor have a major impact on stability, but the input buffer's output impedance has a minor effect on stability. Since Z_B increases with an increase in frequency, it tends to increase stability at higher frequencies.


CFB versus VFB
1-65

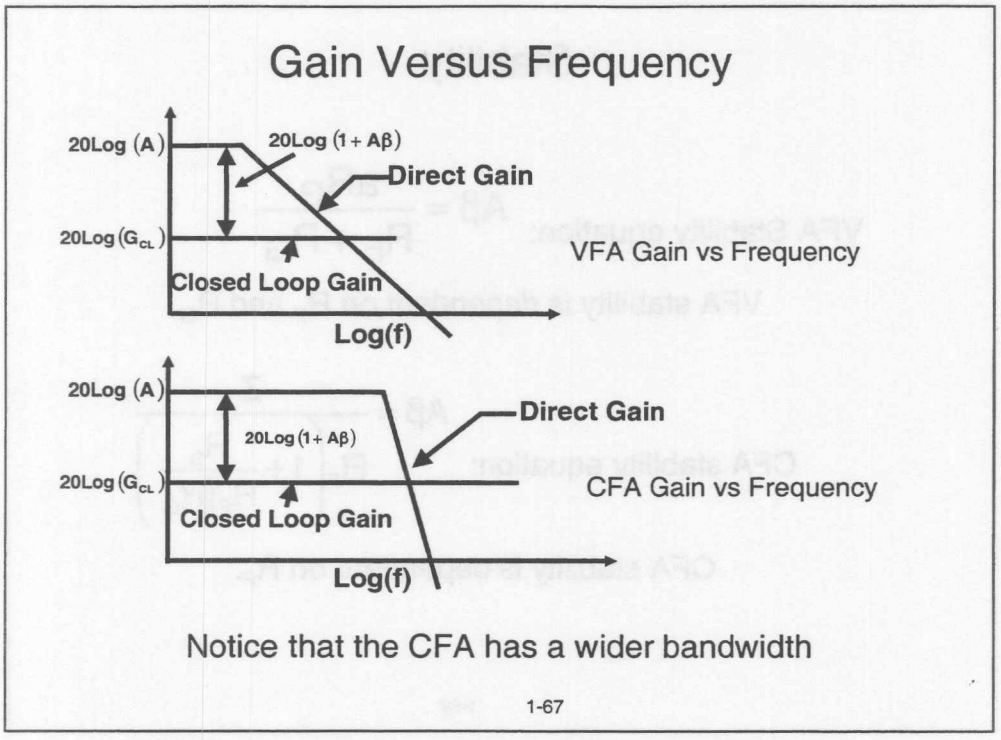
VFA and CFA Comparison

- VFA is highest precision
- CFA is highest speed
- VFA can be a differential amplifier
- Applications overlap at 20 to 100MHz
- VFA has constant GBW limitation
- CFA is more sensitive to stray capacitance
- CFA input impedance is not balanced

1-66

The VFA input stage is a differential amplifier constructed from a long-tailed pair consisting of emitter connected input transistors fed by a common current source. This construction is symmetrical thus it inherently lends itself to precision performance by virtue of matching. The CFA inputs connected to a buffer input and output, thus it is impossible for the CFA to take advantage of matching. The CFA inputs are at dramatically different impedance levels because they are connected to the input and output of a buffer, and this situation precludes operation as a differential amplifier.

The VFA transfer function has a constant gain-bandwidth limitation, and this limitation causes the VFA open loop gain to fall off rapidly after the first pole. The CFA does not have the constant gain-bandwidth limitation, so its open loop gain stays high longer. The CFA's very high frequency response makes it susceptible to any stray capacitance. Present day VFAs can operate at 100MHz, so the applications for these types of op amps tend to overlap in the 20 to 100MHz range.



The VFA has a dominant pole that appears at low frequencies. The dominant pole causes the VFA open loop gain to decrease at a –20dB/decade rate from the pole frequency, and the open loop gain lost by this action can not be used for circuit gain.

The CFA does not have a dominant pole, so its open loop gain does not roll off until much higher frequencies. This enables the CFA to operate at higher frequencies with less error than the VFA.

Stability

VFA Stability equation: $$A\beta = \frac{aR_G}{R_F + R_G}$$

VFA stability is dependent on R_F and R_G.

CFA stability equation: $$A\beta = \frac{Z}{R_F\left(1 + \frac{R_B}{R_F \| R_G}\right)}$$

CFA stability is dependent on R_F.

1-68

Both stability equations are the circuit loop gain equations, Aβ, but the value of Aβ is different for each circuit because the VFA and CFA internal circuitry is different. The VFA stability equation contains R_F and R_G, both of which determine the closed loop gain. Thus, there is no way to change the VFA closed loop gain without impacting the stability.

The CFA stability equation only contains R_F (when R_B is neglected), so R_F is the only external component that determines stability. This gives the CFA another degree of freedom because R_F can be adjusted for stability without affecting the closed loop gain. Also, There is always a value of R_F that stabilizes the circuit. Any capacitance in parallel with R_F destabilizes the circuit because the capacitive impedance decreases to an unstable value at high frequencies. This is why a feedback capacitor should not be used with a CFA.

VFA and CFA Gain Equations

Circuit Configuration	Current Feedback Amplifier (CFA)	Voltage Feedback Amplifier (VFA)
Closed Loop Gain NONINVERTING	$1+\frac{Z_F}{Z_G}$	$1+\frac{Z_F}{Z_G}$
Ideal Loop Gain	$\frac{Z}{Z_F}\left(1+\frac{Z_B}{Z_F \parallel Z_G}\right)$	$\frac{aZ_G}{(Z_G+Z_F)}$
Closed Loop Gain INVERTING	$-\frac{Z_F}{Z_G}$	$-\frac{Z_F}{Z_G}$

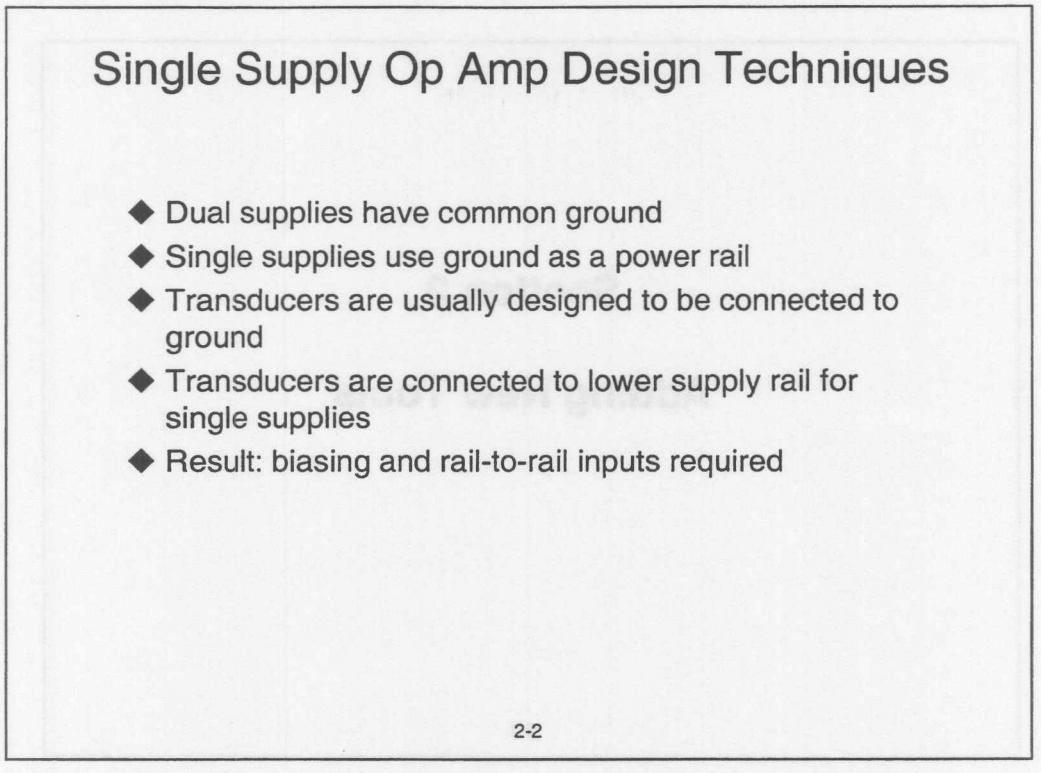
1-69

The ideal closed loop gain equations for the CFA and VFA are identical. The VFA assumes that the op amp gain, a, is very large to arrive at the ideal closed loop gain equation. The CFA arrives at the ideal closed loop gain equation by assuming that the transimpedance, Z, is very large and the input buffer output impedance, R_B, is very small.

Section 2

Adding New Tools

2-1



Single Supply Op Amp Design Techniques

Ground is the common connection between power supplies in dual or split supply op amp circuits. An easy design method for dual supply op amp circuits is to connect the reference input to ground, and then the transducer output voltage can swing above and below ground. Also, if the transducer output voltage swing needs amplification it is small, thus it doesn't exceed the input voltage range of the op amp. No biasing is required is this situation, and the circuit design is simple.

Ground in a single supply op amp circuit is a supply rail, thus when the transducer is connected to ground it is effectively connected to the negative supply rail. Biasing is required to center the output voltage or position it for the next stage. Designing a circuit that has both bias and amplification is significantly harder because the parameters interact, i. e., the need for a surefire single supply design procedure.

Advantages/Disadvantages

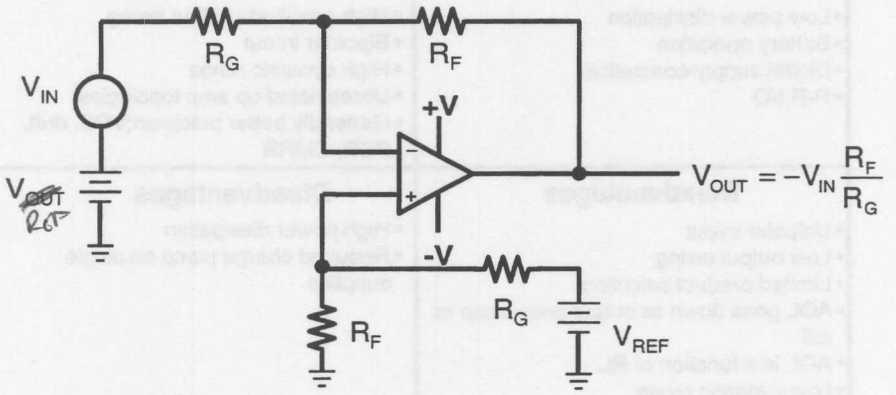
Low Voltage Single Supply	High Voltage Dual Supply
Advantages • Low power dissipation • Battery operation • Digital supply-compatible • R-R I/O	**Advantages** • High amplitude In/Out swing • Bipoloar in/out • High dynamic range • Unrestricted op amp topologies • Generally better precision;VOS, drift, PSR, CMRR
Disadvantages • Unipolar in/out • Low output swing • Limited product selection • AOL goes down as output goes close to rail • AOL is a function of RL • Low dynamic range • Restricted circuit topologies, i.e., no internal integrator, etc. without +VCC/2 bias	**Disadvantages** • High power dissipation • Required charge pump on single supplies

2-3

Both single supply and dual supply op amp designs have advantages and disadvantages. Many designs require a single supply, others do not. When a choice exists the designer should be aware and avoid unnecessary problems as a result of single supply designs.

Dual Supply Op Amps

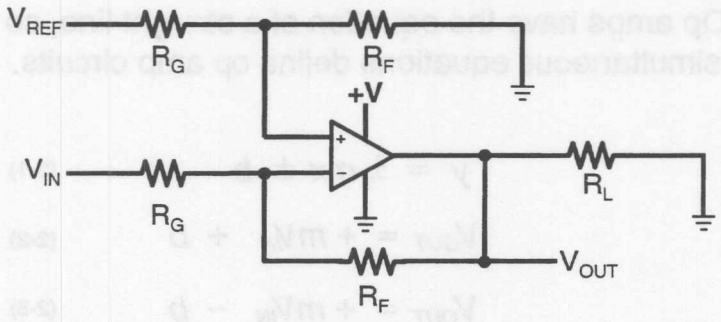
Dual supply circuit with two reference voltages



2-4

The dual or split supply circuit shown includes two reference supplies. When the reference supplies are equal the common-mode rejection capability of the op amp rejects them, and they don't appear in the transfer function. If the reference supplies are not equal the difference voltage is multiplied by the stage gain. When both reference supplies equal zero the circuit reduces to an inverting op amp that has its input referenced to ground.

Single Supply Circuit



$$V_{OUT} = V_{REF}\left(\frac{R_F}{R_G + R_F}\right)\left(\frac{R_F + R_G}{R_G}\right) - V_{IN}\frac{R_F}{R_G}$$

$$V_{OUT} = (V_{REF} - V_{IN})\frac{R_F}{R_G}$$

2-5

This inverting op amp has an inverting signal and non-inverting reference voltage. The reference voltage can be adjusted to cancel any bias in the inverting input signal. The operational range of the circuit is limited because the output voltage can not swing negative. If $R_F = R_G$ and $V_{REF} > V_{IN}$ the output voltage is positive and obtainable. If ($V_{REF} - V_{IN}$) becomes negative the output voltage saturates at ground because the op amp output voltage can't go negative.

Simultaneous Equations

Op amps have the equation of a straight line, so simultaneous equations define op amp circuits.

$$y = \pm mx \pm b \quad (2\text{-}1)$$

$$V_{OUT} = +mV_{IN} + b \quad (2\text{-}2)$$

$$V_{OUT} = +mV_{IN} - b \quad (2\text{-}3)$$

$$V_{OUT} = -mV_{IN} + b \quad (2\text{-}4)$$

$$V_{OUT} = -mV_{IN} - b \quad (2\text{-}5)$$

2-6

The only transfer function that an op amp can have is the equation of a straight line (equation 2-1). There are four possible combinations of the equation of a straight line, and these combinations are given in equations 2-2 through 2-5. A straight line is defined by two data points commonly identified as X1, Y1 and X2, Y2 in mathematical terms. When the straight line defines an op amp transfer function the data points are labeled V_{IN1}, V_{OUT1} and V_{IN2}, V_{OUT2}. Normally, V_{IN} is the op amp input voltage (the transducer output voltage), and V_{OUT} is the op amp output voltage (the next stage's (often an ADC) input voltage).

Simultaneous Equations-Example

Data: $V_{OUT} = 1V$ @ $V_{IN} = 0.1V$ and $V_{OUT} = 4V$ @ $V_{IN} = 0.2V$

$$1 = m(0.1) + b \quad (2\text{-}6)$$

$$4 = m(0.2) + b \quad (2\text{-}7)$$

$$2 = m(0.2) + 2b \quad (2\text{-}8)$$

$$b = -2 \quad (2\text{-}9)$$

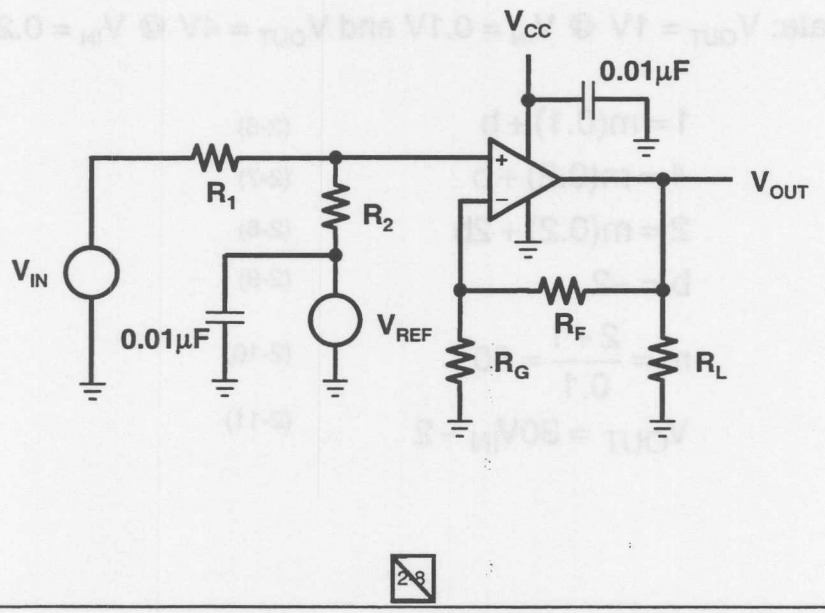
$$m = \frac{2+1}{0.1} = 30 \quad (2\text{-}10)$$

$$V_{OUT} = 30V_{IN} - 2 \quad (2\text{-}11)$$

2-7

The two data points are put into simultaneous equations as shown in equations 2-6 and 2-7. The simultaneous equations are solved to obtain the slope, m, and the vertical intercept, a. The sign of the slope, m, and vertical intercept, a, determines what form of equation 2-1 solves the problem. Then the magnitude of these values is substituted into one of the equations, 2-2 through 2-5, to obtain the final circuit equation. The final solution entails finding a circuit that yields an equation with identical form and determining what component values yield an identical solution.

Case 1: Schematic $V_{OUT} = mV_{IN} + b$



The circuit shown is the simplest one that yields the first quadrant transfer function (case 1). The capacitor across the power supply insures that the ac impedance is very low, and the capacitor across the reference supply strips noise off that supply. Equation 2-12 describes the circuit transfer function.

Case 1: Equations $V_{OUT} = mV_{IN} + b$

$$V_{OUT} = V_{IN}\left(\frac{R_2}{R_1+R_2}\right)\left(\frac{R_F+R_G}{R_G}\right) + V_{REF}\left(\frac{R_1}{R_1+R_2}\right)\left(\frac{R_F+R_G}{R_G}\right) \quad (2\text{-}12)$$

$$V_{OUT} = mV_{IN} + b \quad (2\text{-}13)$$

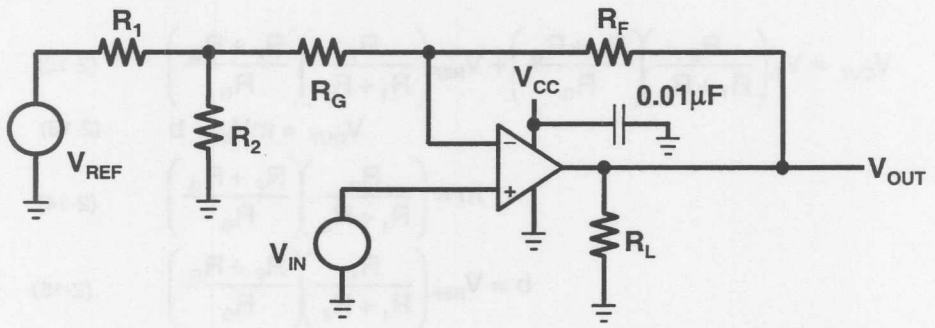
$$m = \left(\frac{R_2}{R_1+R_2}\right)\left(\frac{R_F+R_G}{R_G}\right) \quad (2\text{-}14)$$

$$b = V_{REF}\left(\frac{R_1}{R_1+R_2}\right)\left(\frac{R_F+R_G}{R_G}\right) \quad (2\text{-}15)$$

2-9

Equations 2-14 and 215 equate coefficients between equation 2-12 and the final transfer function. Solving equations 2-14 and 2-15 yields the resistor values for the final circuit.

Case 2: Schematic $V_{OUT} = mV_{IN} - b$



2-10

The circuit shown is the simplest one that yields the second quadrant transfer function (case 2). The capacitor across the power supply insures that the ac impedance is very low. Equation 2-16 describes the circuit transfer function.

Case 2: Equations $V_{OUT} = mV_{IN} - b$

$$V_{OUT} = V_{IN}\left(\frac{R_F + R_G + R_1 \| R_2}{R_G + R_1 \| R_2}\right) - V_{REF}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F}{R_G + R_1 \| R_2}\right) \quad (2\text{-}16)$$

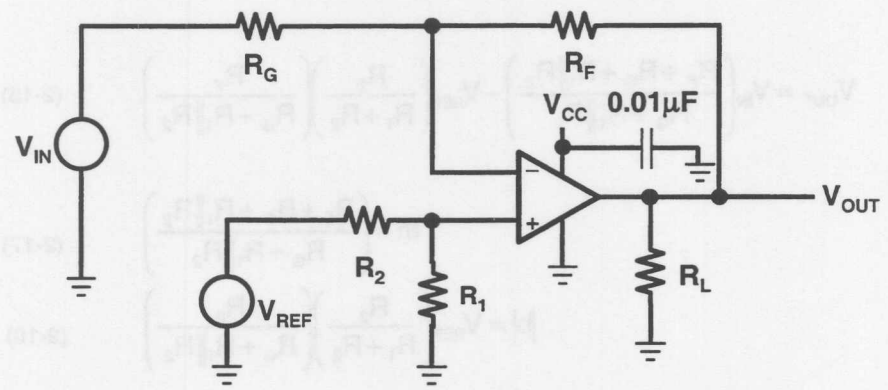
$$m = \left(\frac{R_F + R_G + R_1 \| R_2}{R_G + R_1 \| R_2}\right) \quad (2\text{-}17)$$

$$|b| = V_{REF}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F}{R_G + R_1 \| R_2}\right) \quad (2\text{-}18)$$

2-11

Equations 2-17 and 2-18 equate coefficients between equation 216 and the final transfer function. Solving equations 2-17 and 2-18 yields the resistor values for the final circuit.

Case 3: Schematic $V_{OUT} = -mV_{IN} + b$



Add 0.01µF decoupling cap from V_{CC} to ground

2-12

The circuit shown is the simplest one that yields the third quadrant transfer function (case 3). The capacitor across the power supply insures that the ac impedance is very low. A second capacitor is often connected in parallel with R_1 to shunt reference voltage noise to ground. Equation 2-19 describes the circuit transfer function.

Case 3: Equations $V_{OUT} = -mV_{IN} + b$

$$V_{OUT} = -V_{IN}\left(\frac{R_F}{R_G}\right) + V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \quad (2\text{-}19)$$

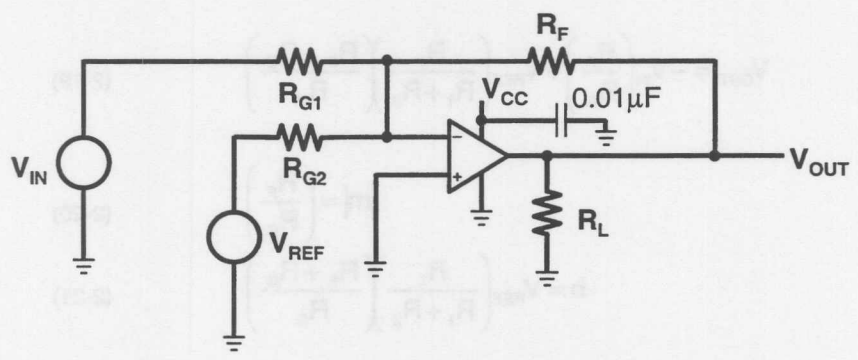
$$|m| = \left(\frac{R_F}{R_G}\right) \quad (2\text{-}20)$$

$$b = V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \quad (2\text{-}21)$$

2-13

Equations 2-20 and 2-21 equate coefficients between equation 2-19 and the final transfer function. Solving equations 2-20 and 2-21 yields the resistor values for the final circuit. The final circuit often employs a protective diode from the negative input (cathode) to ground to protect this input when the op amp power is off and the interface power is on.

Case 4: Schematic $V_{OUT} = -mV_{IN} - b$



2-14

The circuit shown is the simplest one that yields the fourth quadrant transfer function (case 4). The capacitor across the power supply insures that the ac impedance is very low. Equation 2-22 describes the circuit transfer function.

Case 4: Equations $V_{OUT} = -mV_{IN} - b$

$$V_{OUT} = -V_{IN}\left(\frac{R_F}{R_{G1}}\right) - V_{REF}\left(\frac{R_F}{R_{G2}}\right) \quad (2\text{-}22)$$

$$|m| = \left(\frac{R_F}{R_{G1}}\right) \quad (2\text{-}23)$$

$$|b| = V_{REF}\left(\frac{R_F}{R_{G2}}\right) \quad (2\text{-}24)$$

Equations 2-23 and 2-24 equate coefficients between equation 2-22 and the final transfer function. Solving equations 2-23 and 2-24 yields the resistor values for the final circuit. Depending on the relative values of V_{IN} and V_{REF} and their power up status, a protective diode may be need to be connected from the negative input (cathode) to ground.

Rail-to-Rail Input/Output RRIO

- Transducer connected to the power rail require RRI op amps to function
- The op amp input must allow voltages (200mV) beyond the rail to function
- RRI op amps have dual input circuits
- RRIO op amps have maximum output swing to achieve maximum dynamic range

2-16

When transducers are connected to a power rail a special op amp is required because the input voltage swing is so high. The transducer output voltage swings both positive and negative, so when it is connected to a power rail the op amp input voltage exceeds the power supply voltage. This situation may destroy some op amps, and the data is distorted in other op amps, but RRI op amps handle this situation with ease.

The RRI op amp's input voltage range is usually 200mV greater than the power supply, thus power rail connected transducers can be safely used with RRI op amps. If the input voltage swing only includes one power rail PNP input op amps can be used for ground connected transducers and NPN input op amps can be used for power rail connected transducers. RRI op amps usually include RRO to achieve the best possible dynamic range.

Selected Op Amps

Single Supply Op Amps

PART	Notes	S, D, Q	OFFSET (mV) Max	DRIFT (uV/C) Typ	Ib (pA) Max	NOISE 1kHz nV/rtHz	GBW (MHz) Typ	SR (V/us) Typ	Vsup	Iq/Amp (mA) Max	$$ in 1000s
Single Supply – PRECISION (OFFSET < 500μV, LOW DRIFT)											
OPA*y*336	**RRO**, SOT23	S, D, Q	**0.125**	**1.5**	10	40	0.1	0.03	2.3 to 5.5	**0.032**	**$ 0.60**
OPA*y*340	**RRIO**, SOT23	S, D, Q	**0.5**	**2.5**	10	25	**5.5**	6	2.5 to 5.5	0.95	**$ 0.66**
OPA*y*350	**RRIO**, MSOP	S, D, Q	**0.5**	**4**	10	**8**	**38**	**22**	2.5 to 5.5	7.5	**$ 1.22**
Single Supply – WIDE BANDWIDTH & LOW VOLTAGE											
TLV278*x*	**RRIO**, SOT23, SD	S, D, Q	3	8	15	18	**8**	4.2	**1.8** to 4	**0.77**	**$0.59**
TLV277*x*	**RRO**, SOT23, SD	S, D, Q	2.5	2	100	17	**5.1**	**10.5**	**2.2** to 5.5	2	**$0.60**

y: Single=No Number, Dual=2, Quad=4
x: Single=1 (w/SD=0), Dual=2 (w/SD=3), Quad=4 (w/SD=5)

2-17

Matching Op Amp BW to Specifications

- Problem- op amp gain decreases as frequency increases thus increasing errors
- Need to know input signal frequency content
- Calculate or measure signal degradation due to decreasing gain

2-18

There are two problems that occur when the signal and op amp bandwidth (BW) is not matched. When the signal BW exceeds the op amp BW the signal is distorted when amplified by the op amp. When the op amp BW exceeds the signal bandwidth the excess BW amplifies noise and no signal. The moral is that the signal and op amp BW should be matched with the op amp BW being slightly greater than the signal BW. The op amp BW must be greater than the signal BW to allow for worst case conditions, and this situation allows some noise amplification under nominal and best case conditions.

When the signal BW is known it should be tested to find out how much distortion results from amplifier gain roll off. Then the op amp can be selected by matching its gain roll off to the signal. This procedure only accounts for signal distortion due to amplifier gain roll off; dc input offset voltages and currents and other error sources must still be considered.

Input Frequency Signal Content

- Divide signal into segments and take Fourier series
- Measure frequency content of signal with wave analyzer or equivalent instruments
- Put signal through a variable cutoff low pass filter and measure distortion with instrumentation, ear, eye, etc.

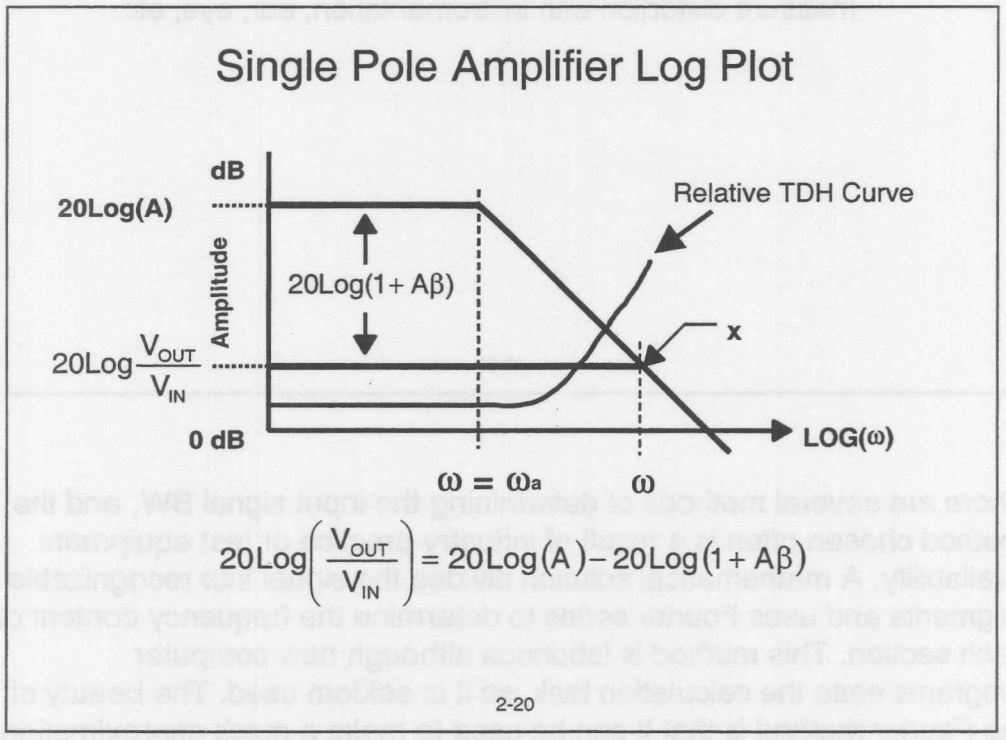
2-19

There are several methods of determining the input signal BW, and the method chosen often is a result of industry practice or test equipment availability. A mathematical solution divides the signal into recognizable segments and uses Fourier series to determine the frequency content of each section. This method is laborious although new computer programs ease the calculation task, so it is seldom used. The beauty of the Fourier method is that it can be used to make a quick approximation with having any hardware.

Another method of determining the signal BW is to measure it with instruments. This method may be more accurate than the Fourier series method, but statistical techniques must be used to account for worst case conditions. The upside of this technique is the lack of interpretation of the results because you see exactly what the signal frequency content is. This is just a laboratory Fourier series.

See Errata

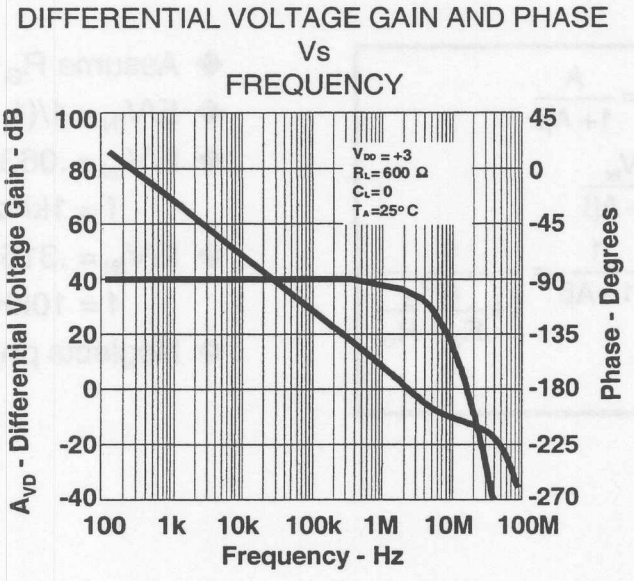
Another method is to put the signal into a variable low pass amplifier while measuring the distortion of the filtered signal. Start at the highest frequency and keep lowering –3dB point of the filter until you measure unacceptable distortion. Now, you have to increase he BW some to get to acceptable distortion and allow for worst case, and the amount of the increase is a judgement factor. Sometimes this technique is used with the final system such as video rather than a distortion analyzer. It can be very hard to correlate distortion to the video, so a system check and testing is always in order.



The amplifier plotted assumes a single pole in the feedback loop, and this is realizable over a good part of the BW. Most amplifiers have multiple poles, but they can be compensated to act like a single pole. Internally compensated op amps act like they have a single pole, and non-internally compensated op amps can use external compensation to achieve the same result.

Notice that until the frequency ω_a occurs the amplifier response is flat and the error is constant. At ω_a the amplifier gain starts rolling off and the error increases rapidly. At the point X the closed loop gain is down –3dB, so the circuit is not usable.

TLV247X Open Loop Log Plot



2-21

This is an actual op amp open loop transfer curve. The ω_a pole is far to the left of the diagram, so the flat portion of the curve is not shown. Notice that the gain slopes down at –20dB per octave, thus the error must be increasing at the same rate. The phase starts to change radically at 1MHz because the op amp's internal poles are coming into play. This is a dangerous area to work in because these pole locations are subject to movement by temperature and manufacturing variations. This op amp is usable in low gain configuration at 250KHz. Around 250KHz the excess gain (1 + Aβ) is high enough to yield about 10% error for low gain. At higher frequencies you get into the closed loop/open loop intersection problem signified by point X on the previous page.

Calculating the Error

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1+A\beta}$$

$$E = \frac{V_{IN}}{1+A\beta}$$

$$\frac{E}{V_{IN}} = \frac{1}{1+A\beta} = \frac{1}{1+\frac{aR_G}{R_F+R_G}}$$

- Assume $R_G = R_F$
- $E/V_{IN} = 1/(1 + a/2)$
- $E/V_{IN} = .0632\%$ @ f = 1kHz
- $E/V_{IN} = .315\%$ @ f = 10kHz
- Neglects phase affect

2-22

The calculations assume that $R_F = R_G$. The error function for an op amp is given in equation 2-25.

$$\frac{E}{V_{IN}} = \frac{1}{1+A\beta} \qquad (2\text{-}25)$$

The loop gain for an op amp is given in equation 2-26. Equations 2-25 and 2-26 are combined to yield equation 2-27.

$$A\beta = \frac{aR_G}{R_F+R_G} \qquad (2\text{-}26)$$

$$\frac{E}{V_{IN}} = \frac{1}{1+\frac{aR_G}{R_F+R_G}} \qquad (2\text{-}27)$$

Use equation 2.2.3 to calculate the error at a given frequency. For example, at f = 1kHz, a ≈ 70dB. Then $a = 10^{3.5} = 3162.2$, and $E/V_{IN} = 1/1582 = .000632$. And, at 10kHz the gain has rolled off 20dB, so a ≈ 50dB. Then $a = 10^{2.5} = 316.2$, and $E/V_{IN} = 1/315.2 = .00317$. The error at 10kHz is appreciable more than it is at 1kHz. These calculations assume that the feedback signal is in phase with the input signal. This is not strictly true, and as frequency increases the phase change is greater, so this calculation is not reliable beyond about 10% error. The same equations are used to calculate the exact error, but they must account for gain and phase.

BW Considerations

- Voltage feedback OA have constant GBW
- Current feedback OA have better frequency response
- Op amp compensation decreases BW
- OA BW need not be greater than highest signal frequency measured
- Testing required to verify performance

2-23

Voltage feedback op amps have a constant GBW product. The unity GBW is often specified, thus you can start at the unity GBW point (where the 20LogA curve passes through the 0dB axis), and assuming a roll off of –20dB per decade calculate the gain at any other frequency. Current feedback amplifiers are not constrained by a constant GBW product; actually their gain stays constant as frequency increases until it falls off sharply. The CFA is not usable past the gain fall off point.

When an op amp is compensated it becomes more stable, but with many types of compensation the open loop BW is decreased. The op amp bandwidth should be slightly larger than the application requires because excess BW just amplifies noise. VFAs often employ a feedback capacitor to eliminate excess BW. CFAs sometimes have an internal compensation point brought out to a lead to enable BW reduction. As in all analog electronic designs, through testing is required.

High Frequency Amplifiers

- Stray capacitance causes instability and poor performance
- No compensation yields better performance than the uncompensated amplifier
- Phase shift must be monitored because it causes distortion and controls stability
- Always consider the load during calculations

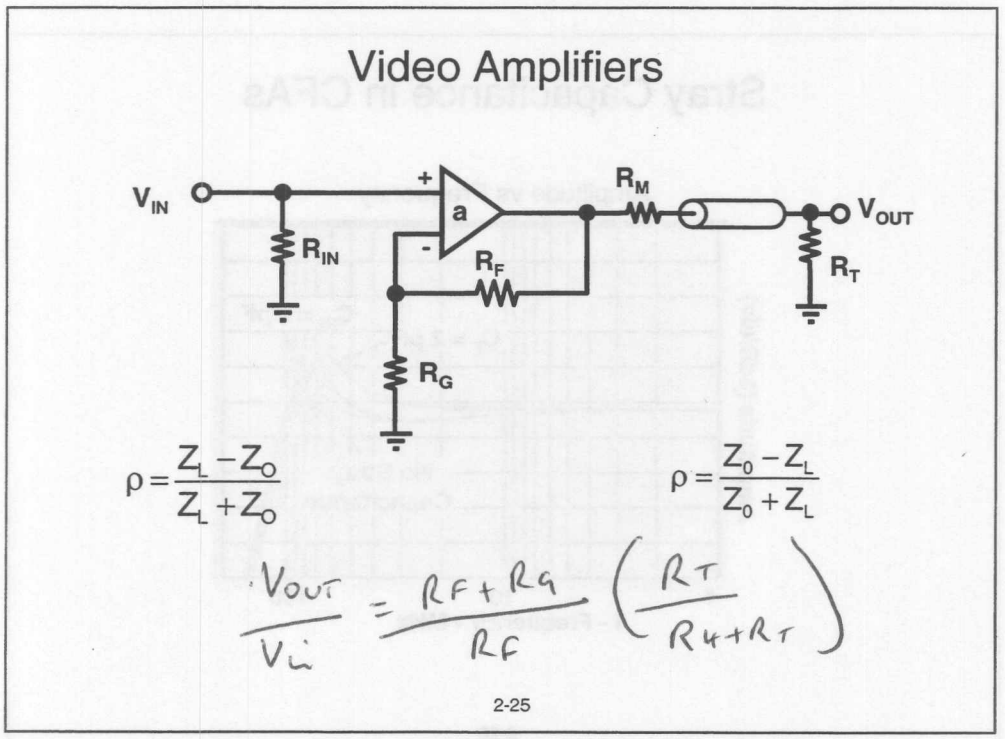
2-24

High Frequency Amplifiers

The layout of high frequency amplifiers is critical because a few pF of capacitance can cause overshoot, ringing, instability, peaking, or BW loss depending on the circuit type and location of the stray capacitance. Stray capacitance on the input node of a VFA tends to cause overshoot, ringing, or instability depending on the value of the stray, where the same stray capacitance causes peaking in a CFA.

When an amplifier exhibits unstable tendencies you must compensate the amplifier to restore stability. Compensation always reduces the closed loop bandwidth to less that that of the uncompensated amplifier. Engineers attempt to increase the BW of an amplifier by bypassing it with a capacitor, and although this trick has some validity, it is not compensation.

A phase-modulated signal is distorted by amplifier phase shift, but excessive phase shift also causes distortion in complex time domain signals. Minimizing phase shift in the signal BW is always a prudent option to incurring phase distortion. The HF amplifier load is very often small because the cable terminating impedance is small (100 to 300Ω), so the load resistance interacts with the amplifier output resistance to form a voltage divider. If the load resistance is too low the selected amplifier may not be able to drive it resulting in the loss of slew rate, output voltage swing, or distortion.



Video amplifiers are terminated in the cable's characteristic impedance that is usually 50Ω, 75Ω, or 100Ω. R_{IN} is the terminating resistor for the previous stage, and it doesn't enter into the calculations. R_M matches the cable impedance to the driver (op amp output circuit). Per equation 2-28, when $R_M = Z_L = Z_O$ the reflection coefficient, ρ, is zero and there are no reflections from the driver.

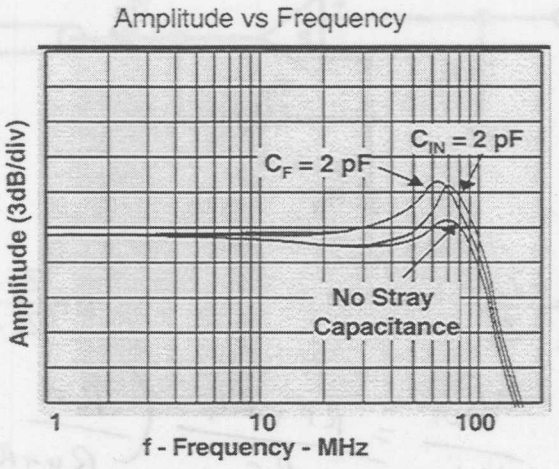
$$\rho = \frac{Z_L - Z_O}{Z_L + Z_O} \qquad (2\text{-}28)$$

The terminating resistor, R_T, (usually located on another circuit board at the cable end) matches the cable to the next amplifier input. Per equation 2-29, when $R_T = Z_L = Z_O$ the reflection coefficient, ρ, is zero and there are no reflections from the end of the receiver.

$$\rho = \frac{Z_O - Z_L}{Z_O + Z_L} \qquad (2\text{-}29)$$

When $R_F = R_G$ the amplifier gain is 2, and when $R_M = R_T$ the terminating gain is ½, thus the system gain is 1. This is a popular circuit in the video world.

Stray Capacitance in CFAs



2-26

CFAs have the widest BW, therefore they are the most susceptible to the effects of stray capacitance. Notice that just 2pF of capacitance added from the inverting input to ground or across the feedback resistor causes over 3dB of peaking. The best method of minimizing stray capacitance is to remove the ground plane around these key nodes.

Uncompensated Op Amps

- Consider using uncompensated op amps with gain compensation
- Works well for voltage feedback op amps
- Use high closed loop gain
- High closed loop gain decreases loop gain
- Dominant pole is moved up in frequency a couple of decades

Internally compensated op amps have a pole located at very low frequencies (1 to 100HZ), and that pole causes the op amp gain to fall off at –20dB/decade. The pole, called a dominant pole, decreases the op amp's BW significantly, but it yields a stable circuit. An alternate method of compensating an op amp is to increase the closed loop gain. This method works because the closed loop gain equation is inversely contained in the loop gain. Putting this together it is clear that we can move the dominant pole to a higher frequency to gain BW, and then increasing the closed loop gain moves the Bode intercept down restoring the lost stability.

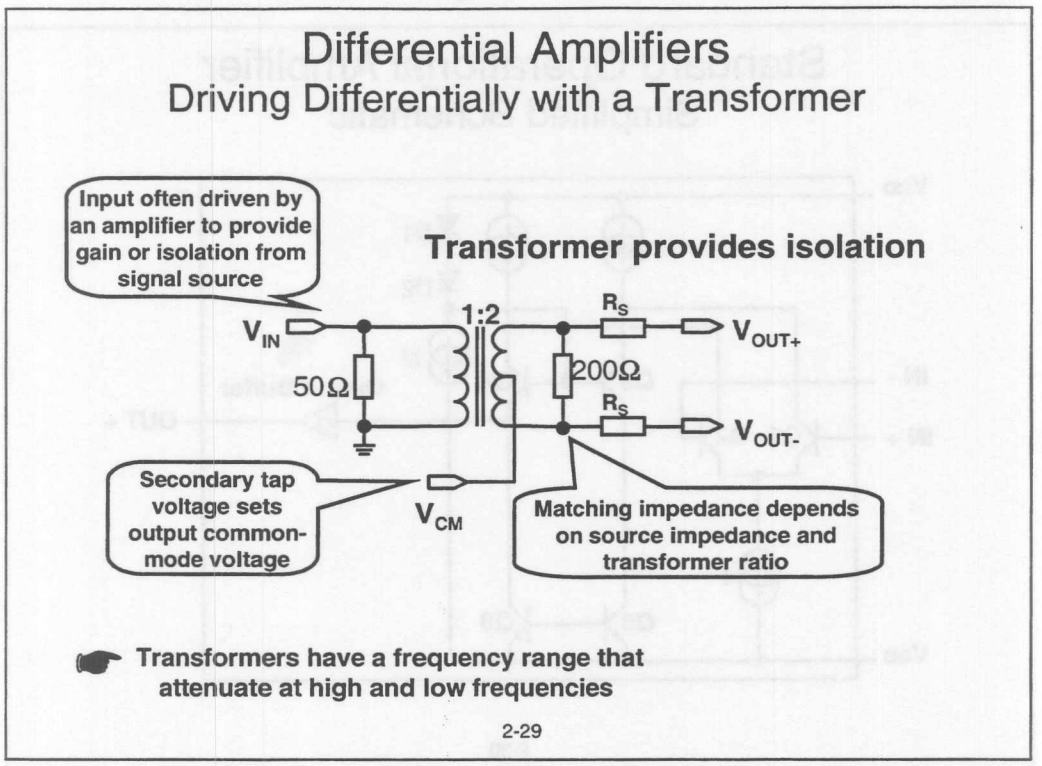
Differential Phase and Gain
Video Specifications

- Gain and phase distortion due to op amp non-linearity
- Differential phase-specifies how much the chrominance phase is affected by the luminance level
- Differential gain-specifies how much the chrominance gain is affected by the luminance level
- Diff gain/phase is specified for HF amps

2-28

Video circuits used in TV applications define two parameters that control the quality of the amplified signal. Differential phase distortion, commonly referred to as differential phase, specifies how much the chrominance phase is affected by the luminance level-in other words, how much hue shift occurs when the luminance level changes. Both positive and negative phase errors may be present, so differential phase is a peak-to-peak measurement. Differential gain distortion, commonly referred to as differential gain, specifies how much the chrominance gain is affected by the luminance level-in other words, how much color saturation shift occurs when the luminance level changes.

See Video Demystified, Keith Jack, HighText, San Diego



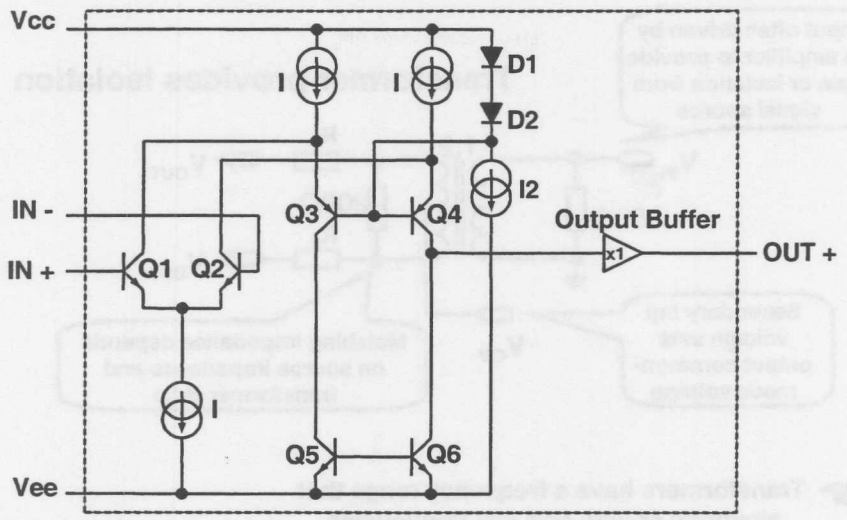
Differential Amplifiers- Driving Differentially with a Transformer

Differential signaling has been commonly used in audio, data transmission, and telephone systems for many years because of its inherent resistance to external noise sources. Two other advantages are reduced even order harmonics and increased dynamic range. Using differential signaling to drive an analog digital converter (ADC) input offers a number of advantages (improved SNR and THD) over a single-ended drive.

One easy way to drive a signal differential is with the use of a transformer. With a transformer a signal-ended or differential signal can be transformed into a differential signal of the required level. The signal size is optimized by the turn ratio of the transformer and the involved termination resistors. On the secondary side of the transformer both ends have a phase difference of 180°. With an applied voltage on the secondary center tap, the common-mode voltage can be set. The advantages that transformers offer are, CMRR that goes on forever, galvanic isolation, no power consumption (efficiencies near 100%), and immunity to very hostile EMC environments. As a drawback, the transformer can only be used for AC application in a defined frequency range.

The alternative solution to the transformer could be a modern differential amplifier if no galvanic isolation is required.

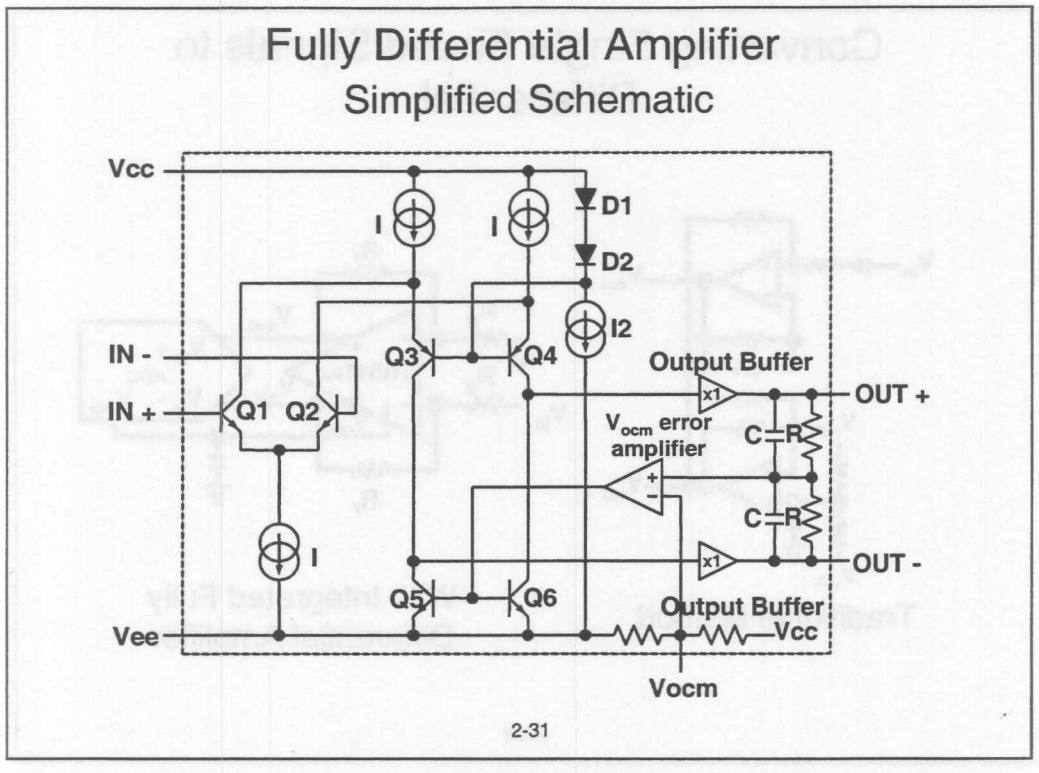
Standard Operational Amplifier
Simplified Schematic



2-30

Amplifier Simplified Schematic

This is a simplified schematic of an op amp with a single ended output. The next figure will illustrate the same amplifier with a differential output.



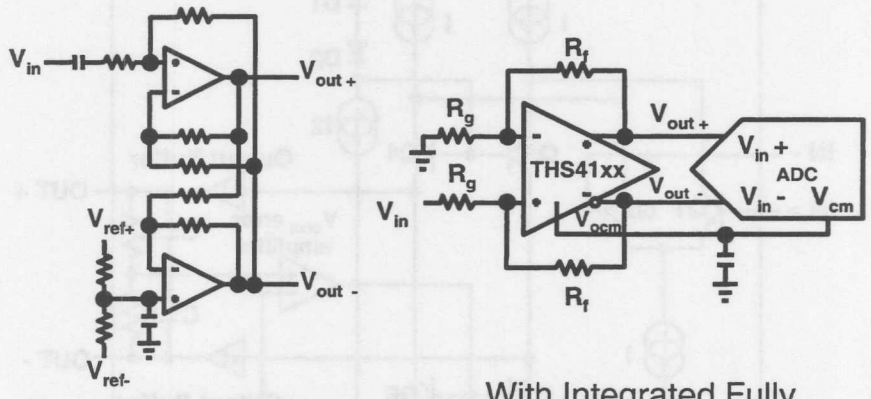
Fully Differential Amplifier Simplified Schematic

An integrated, fully differential amplifier is very similar in architecture to a standard, voltage feedback operational amplifier.

The diagram shows a simplified version of an integrated, fully differential amplifier (representative of the THS4130/1, or THS4140/1). Q1 and Q2 are the input differential pair. In a standard op amp, output current is taken from only one side of the input differential pair and used to develop a single-ended output voltage. In a fully differential amplifier, currents from both sides are used to develop voltages at the high impedance nodes formed at the collectors of Q3/Q5 and Q4/Q6. These voltages are then buffered to the differential outputs OUT + and OUT -.

To first order approximation, voltage common to IN+ and IN- does not produce a change in the current flow through Q1 or Q2 and thus produces no output voltage – it is rejected. The output common-mode voltage is not controlled by the input. The Vocm error amplifier maintains the output common-mode voltage at the same voltage applied to the Vocm pin, by sampling the output common-mode voltage, comparing it to the voltage at Vocm, and adjusting the internal feedback.

Converting Single Ended Signals to Differential



Traditional Method

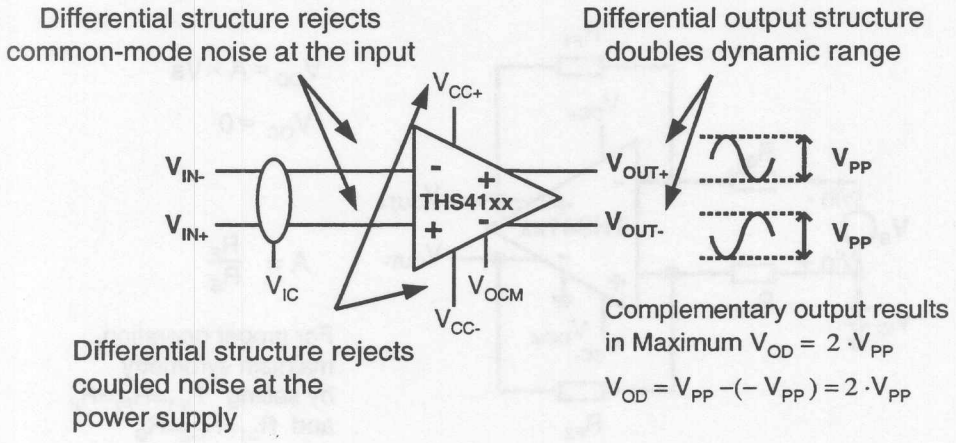
With Integrated Fully Differential Amplifier

2-32

Converting Single Ended Signals to Differential

Converting single ended signals to differential signals to drive high-speed ADCs with differential inputs is a prime application for integrated fully differential amplifiers. In the past, generation of differential signals has been cumbersome. Different means have been used, requiring multiple amplifiers. As can be seen in the diagram, the integrated fully differential amplifier provides a more elegant solution, and reduces the component count.

Fully Differential Amplifier Noise Immunity



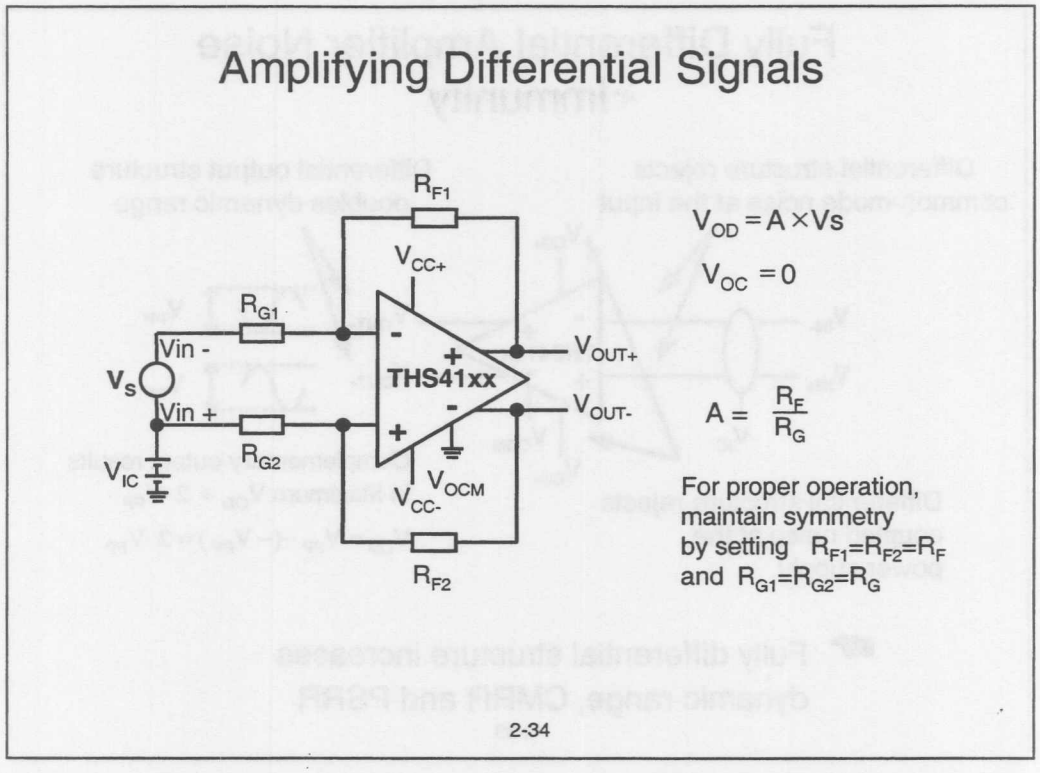
☛ Fully differential structure increases dynamic range, CMRR and PSRR

2-33

Fully Differential Amplifier Noise Immunity

When signals are routed from one place to another, noise is coupled into the circuitry. In a differential system, keeping the transport wires as close as possible to one another (e.g. twisted pair) makes the noise coupled into the conductors appear as a common mode voltage. Noise that is common to the power supplies will also appear as a common mode voltage. Since the differential amplifier rejects common mode voltages, the system is more immune to external noise. The slide above shows the noise immunity of a fully differential amplifier pictorially.

Due to the change in phase between the differential outputs, the dynamic range increases by 6 dB (factor 2) over the SE output with the same voltage swing. Another advantage is reduced even order harmonics



Amplifying Differential Signals

In a fully differential amplifier, there are two feedback paths possible in the main differential amplifier, one for each side. This naturally forms two inverting amplifiers, and inverting topologies are easily adapted to fully differential amplifiers. The diagram shows how to configure a fully differential amplifier with negative feedback to control the gain and maintain a balanced amplifier.

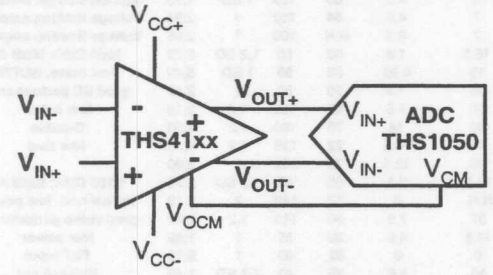
Symmetry in the two feedback paths is important to have good CMRR performance. CMRR is directly proportional to the resistor matching error – 0.1% error results in 60dB of CMRR.

The Vocm error amplifier is independent of the main differential amplifier. The action of the Vocm error amplifier is to maintain the output common-mode voltage at the same level as the voltage input to the Vocm pin. With symmetrical feedback, output balance is maintained, and Vout+ and Vout- swing symmetrically plus and minus from the voltage at the Vocm input.

There is an evaluation module (EVM) available to evaluate the THS4141, refer to part number SLOP345.

Fully Differential Amplifier

Amplifies differential input signals to differential output



Common-Mode Voltage

$$V_{IC} = \frac{V_{IN+} + V_{IN-}}{2}$$

$$V_{OC} = \frac{V_{OUT+} + V_{OUT-}}{2}$$

Input voltage definition	$V_{ID} = V_{IN+} - V_{IN-}$
Output voltage definition	$V_{OD} = V_{OUT+} - V_{OUT-}$
Transfer function	$V_{OD} = A(f) \cdot V_{ID}$
Ouput common-mode voltage	$V_{OC} = V_{OCM}$

☛ **V_{OCM} is required to set output common-mode voltage, V_{OC}**

2-35

Fully Differential Amplifier

The second commonly used method to manipulate differential signals are full Differential Amplifiers. They have advantages, such as low cost, small size and weight, and superior frequency response at low frequency and DC. An integrated fully differential amplifier is very similar in architecture to a standard operational amplifier. To first order approximation, voltage common to IN+ and IN- does not produce a change in output voltage – it is rejected. The output common-mode voltage is not controlled by the input. The internal Vocm error amplifier controls the output common-mode voltage by sampling it, comparing it to the voltage at Vocm, and adjusting the internal feedback.

To understand how a fully differential amplifier behaves, it is important to understand the voltage definitions that are used to describe the amplifier. The slide shows a block diagram used to represent a fully differential amplifier and its input and output voltage definitions. The voltage difference between the plus and minus inputs is the input differential voltage, V_{ID}. The average of the two input voltages is the input common-mode voltage, V_{IC}.

The difference between the voltages at the plus and minus outputs is the output differential voltage, V_{OD}. The output common-mode voltage, V_{OC}, is the average of the two output voltages, and is controlled by a external reference voltage V_{OCM} . A(f) is the frequency dependant differential gain of the amplifier so that : $\mathbf{V_{OD} = A(f) \cdot V_{ID}}$

Voltage Feedback High Speed Amplifiers

Device	G nom	BW@Gnom	SR	Vcc	Icc	t sett	Vnoise	THD	Iout	x	Price	Comments
		[Mhz]	[V/us]	[V]	[mA]	[ns] to 0.1%	nV/rtHz	[dB]	[mA]		$ 1k	
OPA680	1	400	1800	5 - 10	6.4	8	4.8	80	150	1 SD	1.79	high SR voltage feedback
OPA689	4	280	1600	5 - 10	15.8	7	4.6	64	100	1	2.95	Voltage limiting amplifier
OPA688	1	530	1000	5 - 10	15.8	7	6.3	N.N.	100	1	2.65	Voltage limiting amplifier
OPAx643	5	300	1000	10	20.0	16.5	1.8	92	60	1,2 SD	3.75	90dB CMR; 95dB Aol
OPA687	12	600	900	10	18.0	15	0.95	85	80	1 SD	3.49	low noise, SOT23
OPA686	7	250	600	5 - 10	12.0	16	1.3	90	80	1	2.89	good DC performance
THS402x	10	350	470	10 - 30	9.5	10	1.5	68	100	1,2	2.19	low noise
THS404x	1	165	400	10 - 30	9.5	95	14	75	100	1,2	1.65	C-stable
THS406x	1	180	400	10 - 30	7.8	40	14.5	72	115	1,2	1.39	low cost
THS4001	1	270	400	10 - 30	7.8	40	12.5	72	100	1	2.00	
OPAx642	1	450	380	10	20.0	11.5	2.3	95	60	1,2 SD	3.75	90dB CMR; 95dB Aol
OPA2652	1	700	335	6 - 12	5.5	N.N.	8	77	140	2	1.19	lowest cost, low power
THS401x	1	290	310	10 - 30	7.8	37	7.5	80	110	1,2	2.29	good video performance
OPA651	2	470	300	10	5.1	11.5	4.6	80	85	1	1.95	low power
OPA655	1	400	290	10	21.0	6	6	92	60	1	9.13	FET Input
OPAx634/5	1	150	250	2.7 - 10	10	15	5.6	76	80	1,2 SD	1.49	Rail-rail out
THS405x	1	70	240	10 - 30	8.5	60	14	82	100	1,2	1.10	low cost
OPAx650	1	560	240	10	5.1	10.2	8.4	80	85	1,2,4	1.31	low cost
THS408x	1	175	230	10 - 30	3.4	43	10	64	85	1,2	1.79	low current
THS6072	1	175	230	10 - 30	3.4	43	10	79	85	2	2.36	low current XDSL receiver
THS403x	2	100	100	10 - 30	8.5	60	1.6	72	90	1,2	2.04	low noise
THS6062	2	100	100	10 - 30	8.5	60	1.6	72	90	2	2.14	XDSL receiver
OPAx631/2	1	75	100	2.7 - 10	6.0	17	6	54	80	1,2 SD	1.29	Rail-rail out

Fixed Gain Buffers												
Device	G nom	BW@Gnom	SR	Vcc	Icc	t sett	Vnoise	THD	Iout	x	Price	Comments
		[Mhz]	[V/us]	[V]	[mA]	[ns] to 0.1%	nV/rtHz	[dB]	[mA]		$ 1k	
OPAx262	1,-1,2	240	2100	5 -10	6	8	2.2	N.N.	190	1,2,3	1,82	Ideal video buffer, disable

Current Feedback High Speed Amplifiers

Device	G nom	BW	SR	Vcc	Icc	SFDR	THD	Iout	x	Price	Comments
		[Mhz]	[V/us]	[V]	[mA]	[dB]	[dB]	[mA]		$ 1k	
THS3001	-1	420	6500	10.0 - 30	7.5		96	20	1	3.09	highest slew rate available
OPA685	2	900	4200	5.0 - 10	12.9	68		60	1 SD	1.89	SOT23, low distortion
OPAx681	2	220	2100	5.0 - 10	6.0	74		135	1 SD	1.79	
OPAx658	2	900	1900	5.0 - 10	5.0	68		60	1,2,4	1.49	
THS6022	-1	210	1900	10.0 - 30	7.2		66	250	2	2.91	CPE xDSL line driver
THS6012	-1	140	1300	10.0 - 30	11.5		65	500	2	4.85	CO xDSL line driver
THS6032	-1	100	1200	10.0 - 30	3.8		60	500	2	5.09	Class G xDSL line driver
OPA2677	2	200	1100	12	18.0	72		280	2	2.29	CPE xDSL line driver
OPA2607	8	25	600	24	17.0	72		150	2	2.29	CPE xDSL line driver

Sorted by slew rate

Designing Anti-Alias Filters

- Filters are used in telecom for signal ID
- Most data acquisition systems require anti-alias filters
- Power supplies use noise control filters
- Some filters yield a constant time delay
- Active filters do not use inductors

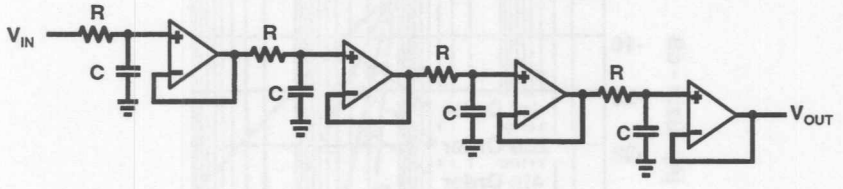
2-38

The Webster definition of a filter is, *A filter is a device that passes electric signals at certain frequencies or frequency ranges while preventing the passage others.* Filters are used in many applications, and one is telecommunications where band-pass (BP) audio is used in modems and BP HF is used for channel selection. Data acquisition usually uses at least one passive filter for anti aliasing, very often it includes an active filter to provide high performance. Filters are also used in power supplies, power lines, interface circuits (especially mechanical interfaces like switches), and data lines.

Anatol I. Zerev, Handbook of Filter Synthesis, Wiley, New York,
ISBN 047 198680 1

Fourth Order Passive RC Low Pass (LP) Filter

Brute force not recommended



$$A(S) = \frac{1}{(1+\alpha_1 s)(1+\alpha_2 s)....(1+\alpha_n s)}$$

If f_c is identical $\alpha = \sqrt[n]{\sqrt{2}-1}$ $\alpha = 2.3$, and $f_{c(actual)} = f_c/2.3$

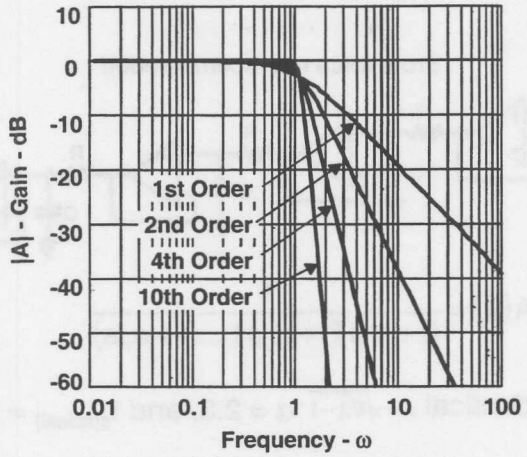
2-39

Passive filters do not cascade well because the output impedance is to high and the input impedance is too low. Passive filters are buffered by op amps to avoid this effect, but the filter roll off frequencies do not add arithmetically. The roll off frequency of n cascaded stages is reduced by the factor:

$$\alpha = \sqrt[n]{\sqrt{2}-1}$$

Butterworth LP Filter

Most Commonly Used Filter

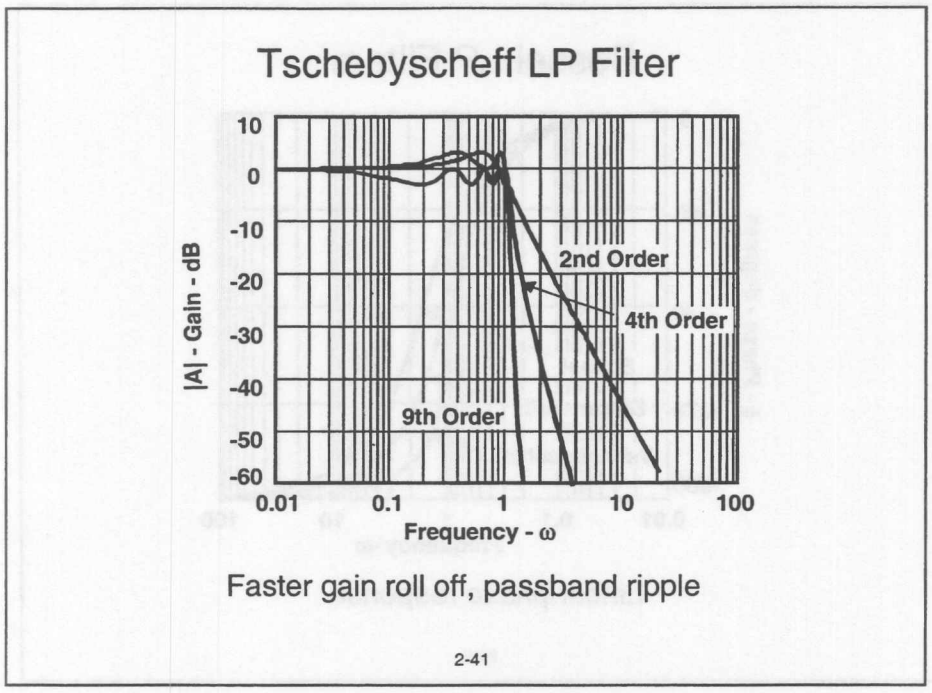


Maximum Passband Flatness

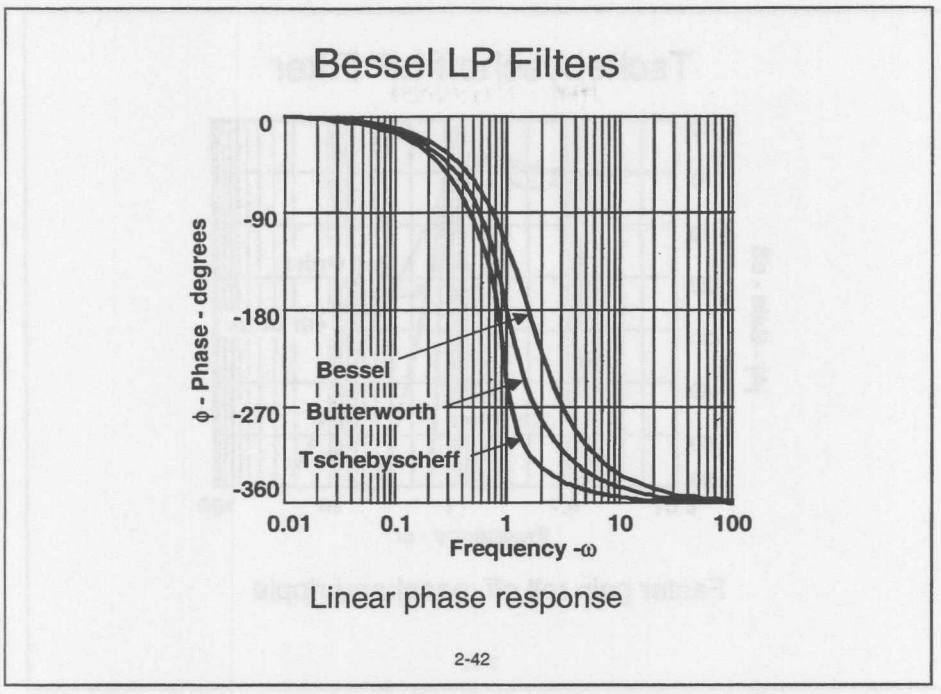
2-40

The Butterworth low pass filter provides maximum passband flatness. Therefore, a Butterworth low pass active filter is often used as an anti aliasing filter in data converter applications where the data is contained in the signal level.

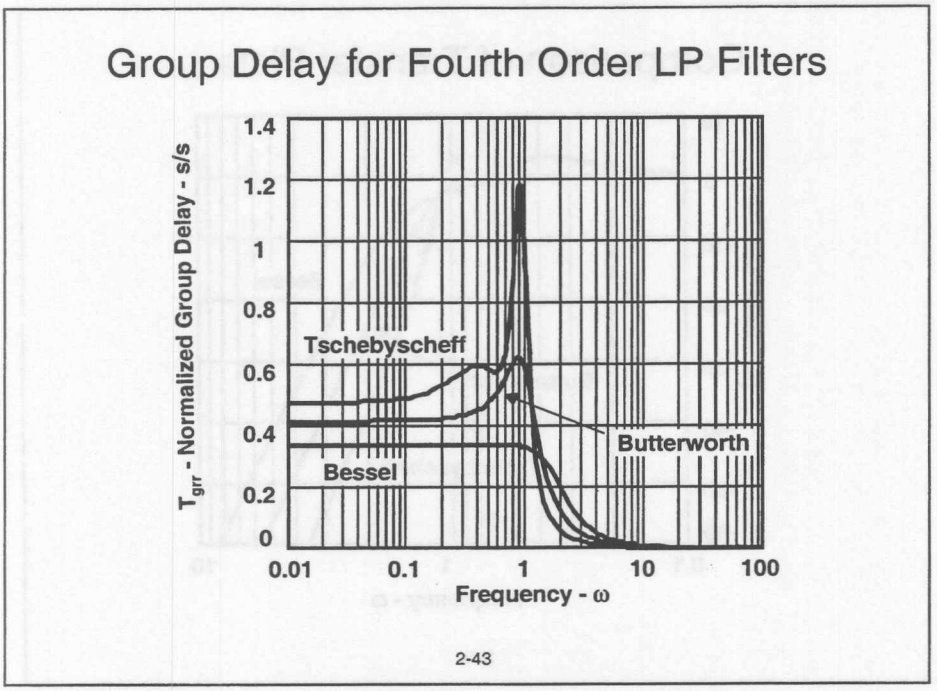
See Errata



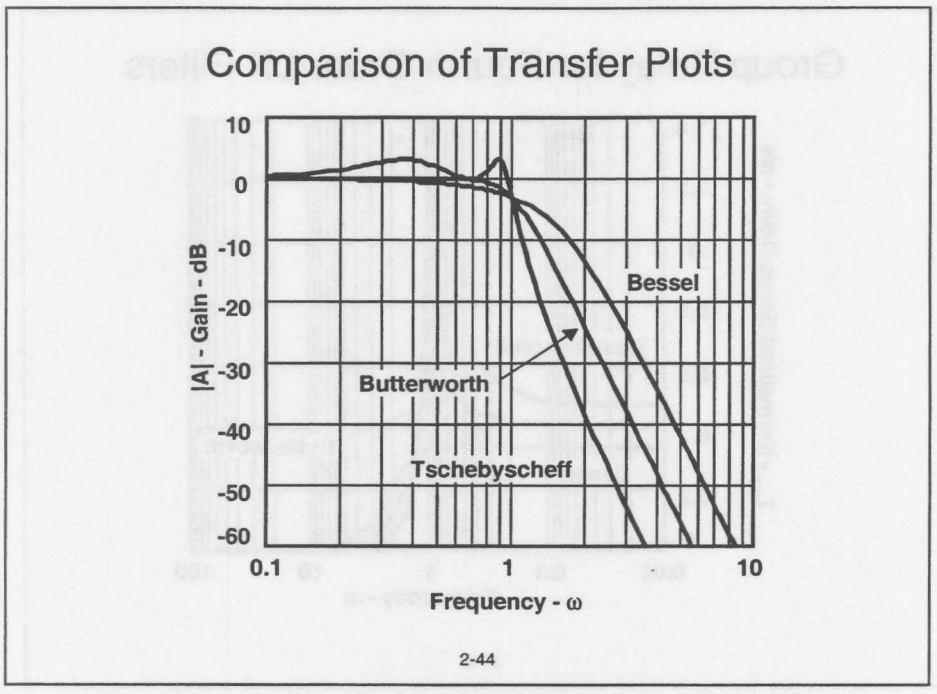
The Tschebyscheff low pass filter has the fastest gain roll off at frequencies higher than f_c, but the passband gain has ripple. As the filter order increases the filter ripple decreases. Filters with even orders generate ripple that appears above the 0dB intercept and filters with odd orders generate ripple below the 0dB intercept. Tschebyscheff filters are often used in multiple section configurations in applications where the frequency content is more important than the amplitude.



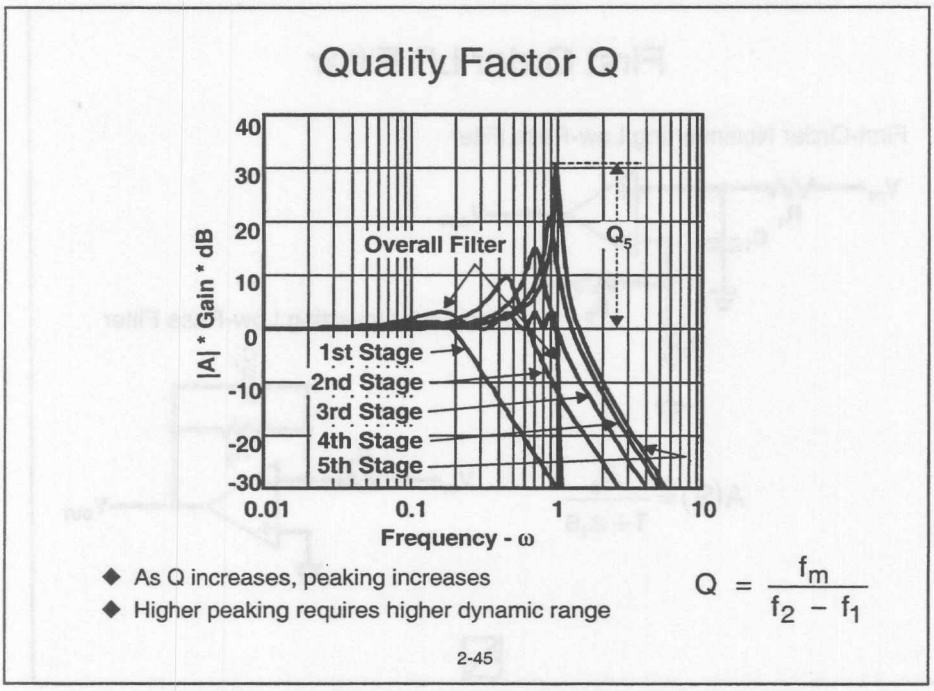
Bessel low pass filters have a linear phase response over a wide frequency range, and this results in a constant group delay within that frequency range. Bessel low pass filters provide the optimum filter for square waves because the square wave component frequencies are delayed equally causing less distortion. The passband gain of a Bessel low pass filter is not as flat as that of a Butterworth low pass filter.



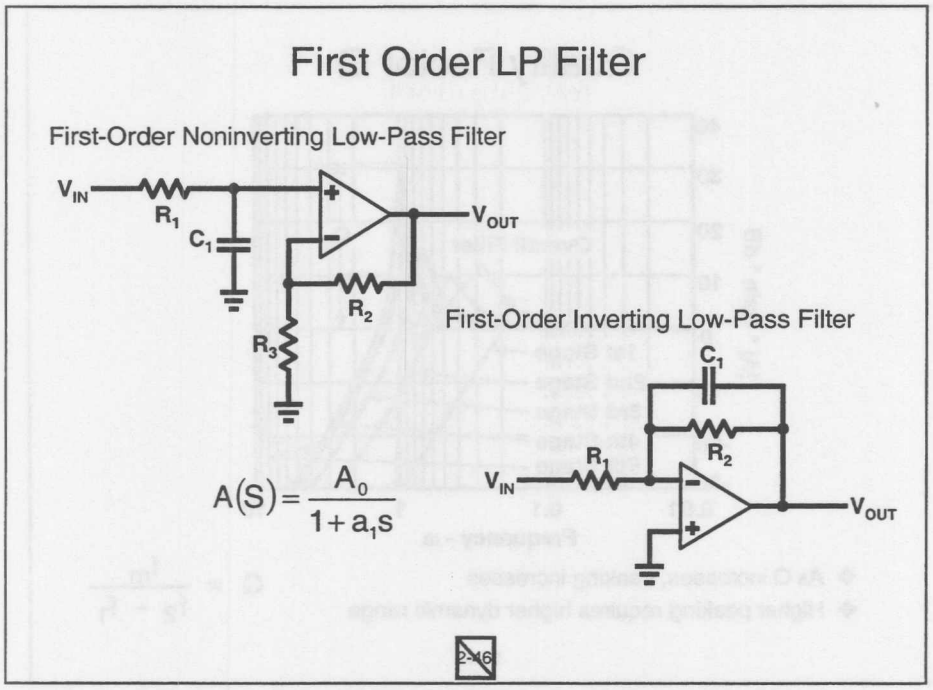
The group delay for Butterworth and Tschebyscheff filter is approximately constant for a decade, and it varies widely at higher frequencies. Both of these filters have wild group delay characteristics around the cutoff frequency. The Bessel filter has a constant group delay until the cutoff frequency, and then the delay decreases to zero exponentially.



The Butterworth low pass filter response is flat at 0dB until it reaches the cutoff frequency. The Tschebyscheff low pass filter exhibits some ripple in the passband. The Bessel low pass filter starts to roll off well before the cut off frequency.



The quality factor and filter order, n, are equivalent design parameters. Rather than designing an n^{th} order Tschebyscheff low pass filter one can design a Tschebyscheff low pass filter with an equivalent Q. In a band pass filter Q is defined as the ratio of the mid band frequency, f_m, to the –3dB bandwidth.



The low pass filter equation is given below.

$$A_i(s)=\frac{A_0}{1+a_is+b_is^2} \qquad (2\text{-}30)$$

The coefficient, b, is equal to zero in a first order filter, so the equation reduces to equation 2-31.

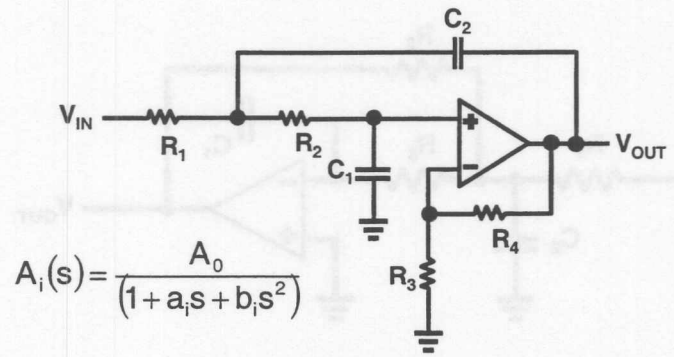
$$A(s)=\frac{A_0}{1+a_1s} \qquad (2\text{-}31)$$

Where:

$$A_{o(INV)}=-\frac{R_2}{R_1} \qquad (2\text{-}32)$$

$$A_{O(NON\text{-}INV)}=1+\frac{R_2}{R_3} \qquad (2\text{-}33)$$

Second Order LP Filter
(Sallen-Key)



$$A_i(s) = \frac{A_0}{(1 + a_i s + b_i s^2)}$$

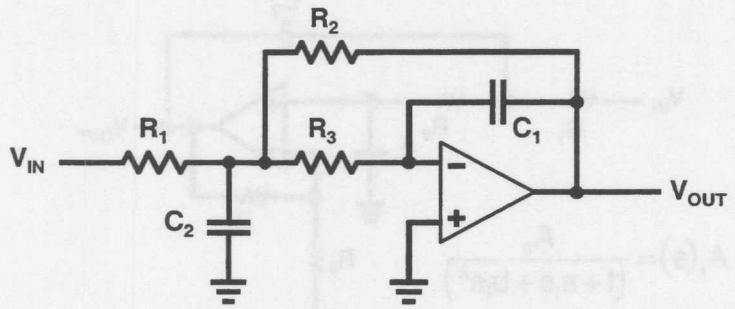
Usually used in applications requiring high accuracy, unity gain, and low Q (Q<3)

2-47

There are two topologies for a second order low pass filter, the Sallen-Key and the Multiple Feedback (MFB) topology. The Sallen-Key topology allows for separate gain setting via $A_0 = (1 + R_4/R_3)$. The unity gain topology (R_4 = 0 and R_3 = open) is usually used in applications requiring high accuracy, unity gain, and low Q (Q<3).

$$A(s) = \frac{A_0}{1 + \omega_C[C_1(R_1 + R_2) + (1 - A_0)R_1C_2]s + \omega_C^2 R_1 R_2 C_1 C_2 s^2} \quad (2\text{-}34)$$

Second Order LP Filter
(Multiple Feedback)



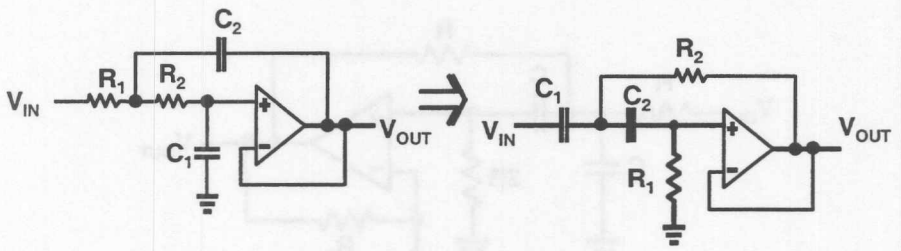
High gain, high Q

2-48

The multiple Feedback topology is used when filters require high gain and high Q.

$$A(s) = -\frac{\frac{R_2}{R_1}}{1 + \omega_C C_1 \left(R_2 + R_3 + \frac{R_2 R_3}{R_1} \right) s + \omega_C^2 C_1 C_2 R_2 R_3 s^2} \qquad (2\text{-}35)$$

Salen-Key High Pass (HP) Filters



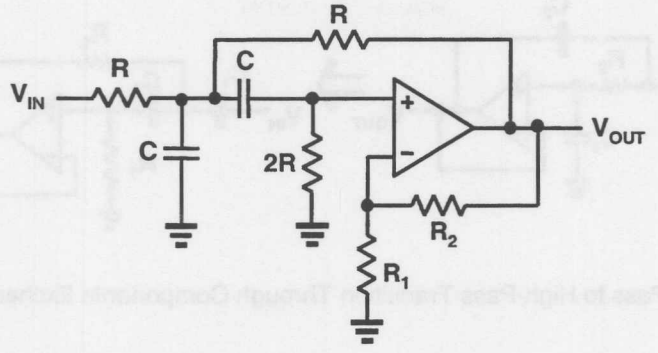
Low-Pass to High-Pass Transition Through Components Exchange

2-49

The low pass filter transforms to the high pass filter when the resistors and capacitors are interchanged. The general equation of a high pass filter is given in equation 2-36.

$$A(s) = \frac{A_\infty}{\prod_i \left(1 + \frac{a_i}{s} + \frac{b_i}{s^2}\right)} \qquad (2\text{-}36)$$

Sallen-Key Band Pass (BP) Filter



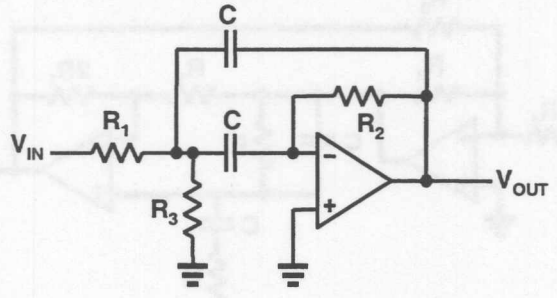
Q and mid band gain cannot be adjusted independently

2-50

The Sallen-key circuit has the advantage that the quality factor, Q, can be varied via the op amp gain without modifying the mid frequency. The Q and mid band gain can not be adjusted independently because the op amp gain ties them together. When the op amp gain approaches 3 the mid band gain becomes infinite causing oscillations.

$$A(s) = \frac{GRC\omega_m s}{1 + RC\omega_m(3-G)s + R^2C^2\omega_m{}^2 s^2} \qquad (2\text{-}37)$$

Multiple Feedback BP Filter



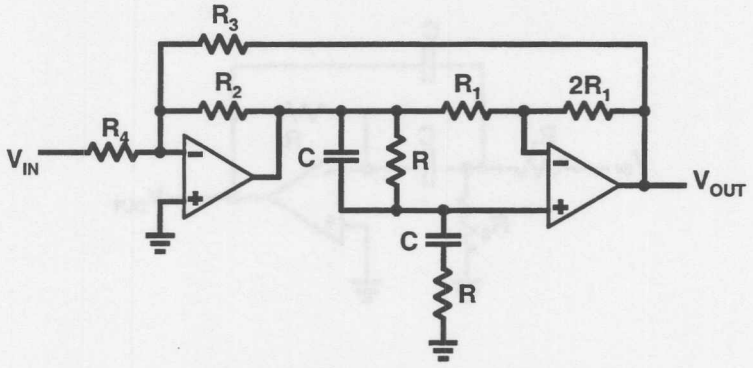
When Q is low, R3 can be eliminated

2-51

The MFB band pass filter enables independent adjustment of Q, mid band gain, and mid band frequency. R_3 can be used to modify the mid band frequency without affecting bandwidth or mid band gain. When the Q is low R_3 can be eliminated, but then Q and mid band gain become interrelated.

$$A(s) = \frac{-\frac{R_2 R_3}{R_1 + R_3} C\omega_m s}{1 + \frac{2R_1 R_3}{R_1 + R_3} C\omega_m s + \frac{R_1 R_2 R_3}{R_1 + R_3} C^2 {\omega_m}^2 s^2} \qquad (2\text{-}38)$$

Wein-Robinson Filter



Can change pass band gain without affecting the Q.

2-52

The Wein-Robinson filter is a bridge band rejection filter. In comparison to the twin T filter, the Wein-Robertson filter enables modification of the pass band gain without affecting the Q. If the mid band frequency is not completely suppressed fine tuning of $2R_2$ should suppress it.

$$A(s) = -\frac{\frac{\beta}{1+\alpha}\left(1+s^2\right)}{1+\frac{3}{1+\alpha}s+s^2} \qquad (2\text{-}39)$$

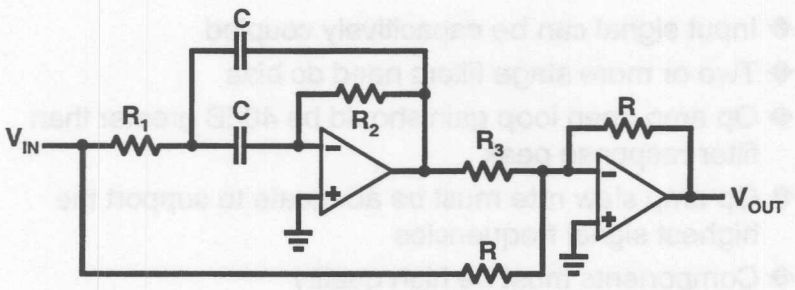
with

$$\alpha = \frac{R_2}{R_3}$$

and

$$\beta = \frac{R_2}{R_4}$$

Second Order All Pass Filter



2-53

An all pass filter has a constant gain across the frequency range, and a phase response that changes linearly with frequency. All pass filters are used in phase compensation and delay circuits.

$$A(s) = \frac{1 + (2R_1 - \alpha R_2)C\omega_C s + R_1 R_2 C^2 \omega_C{}^2 s^2}{1 + 2R_1 C\omega_C s + R_1 R_2 C^2 \omega_C{}^2 s^2} \qquad (2\text{-}40)$$

Biasing and Op Amp Selection

- Input signal can be capacitively coupled
- Two or more stage filters need dc bias
- Op amp open loop gain should be 40dB greater than filter response peak
- Op amp slew rate must be adequate to support the highest signal frequencies
- Components must be high quality

2-54

Input signals can be capacitively coupled into the filter circuit to eliminate the dc component of the input signal. AC coupling also eliminates the requirement for matching two different dc levels. When the filter output voltage swing is defined, as in ADC input signals, biasing may be included in the filter design. Normally when two or more stages are cascaded some biasing is required.

The op amp bandwidth must be 40dB higher than the filter highest frequency to obtain 1% accuracy. Peaking is a natural part of some filter responses, and the 40dB should be measured from the amplitude peak. Also, the op amp slew rate must be faster than the signal's fastest slew rate.

The passive components are an important part of the filter. The components must be stable and have adequate initial tolerances. Also, the frequency response of the components must be much higher than the frequency content of the input signal. Beware of components that have large stray capacitances or leakage.

Selected Op Amps

High-Performance General Purpose
(Supply Voltage >2.5V)

PART	Notes	IIB (pA) Max	OFFSET (mV) Max	NOISE 1kHz nV/rtHz	GBW (MHz) Typ	SR (V/us) Typ	Vsup	Iq/Amp (mA) Max	$$ in 1000s
TLV246*x*	Low Noise, SS, RRIO, SOT23, **SD**	14000	2	**11**	6.4	1.8	2.7 to 6	**0.65**	**$ 0.53**
TLV247*x*	LOW DRIFT, RRIO, **SD**	50	2.2	15	6.4	2	2.7 to 6	0.9	**$ 0.53**
OPA*y*340	SS, RRIO, SOT23	10	**0.5**	25	5.5	6	2.5 to 5.5	0.95	**$ 0.66**
TLV245*x*	SS, SOT23, **SD**		**1.5**	49	**0.29**	0.12	2.7 to 6	**0.034**	**$ 0.53**
TLV27*x*	TLC27x RRO upgrade	50	5	39	3	2.4	2.7 to 15	0.66	$ 0.33
OPAy350		10	0.5	5	38	22	2.7 to 5.5	7.5	$ 1.22
OPAy241		-20000	0.25	45	1035	0.01	2.7 to 36	0.03	$ 1.06

y: Single=No Number, Dual=2, Quad=4
x: Single=1 (w/SD=0), Dual=2 (w/SD=3), Quad=4 (w/SD=5)

2-55

Low Voltage Op Amp Circuits

- Definition-single power supply < 5V
- Reduced dynamic range
- Single supply so bias is required
- Noise is more important
- Op amp drift error more important
- Need RRIO circuits

2-56

By definition, low voltage usually means that there is a single power supply available, and that the power supply voltage is 5V or less. Some battery-powered systems do have split supplies, but they are forced to split the supplies because of sensing or data transmission reasons. Lower voltage, all other parameters held constant, always means lower dynamic range because dynamic range is power supply dependent.

Biasing is usually a circuit design requirement because only a single supply is available. Controlling op amp internal noise becomes more important because the other noise sources tend to decrease with decreasing power supply voltage. Op amp drift subtracts from the dynamic range, thus with reduced dynamic range, the op amp drift must be reduced. Rail-to-rail input and output (RRIO) circuits become popular because the ability to sense and amplify signals connected to the power rails is required in single supply design.

Dynamic Range

$$DR = 20\text{Log}_{10}\left(\frac{V_{OUT(MAX)}}{V_{OUT(MIN)}}\right)$$

$$V_{OUTMAX} = V_{OH(MIN)} - V_{OH(MAX)}$$

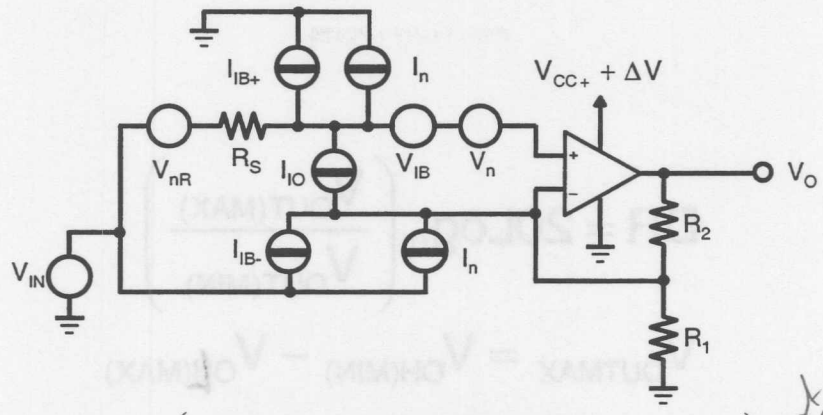
2-57

The dynamic range equation is given below.

$$DR = 20\text{Log}_{10}\left(\frac{V_{OUT(MAX)}}{V_{OUT(MIN)}}\right) \quad (2\text{-}41)$$

The output swing of an op amp is directly dependent on the power supply, thus when the supply voltage decreases the dynamic range decreases. The minimum out voltage of an op amp is not zero, rather it is determined by the error voltages.

Op Amp Error Sources



$$V_{OUT(MIN)} = G_{CL}\left(V_{IO} + I_{IO}R_S + \Delta V_{IO} + \frac{V_{IN} + I_{IB}R_P}{CMRR} + \frac{\Delta V}{k_{SVR}} + V_n + I_nR_{EQ} + I_{nR}R\right)$$

$$DR = 20Log_{10}\left(\frac{V_{OUT(MAX)} - V_{OL(MIN)}}{V_{OUT(MIN)}}\right) = 20Log_{10}\left(\frac{V_{OUT(MAX)}}{V_{OUT(MIN)}}\right)$$

2-58

The major op amp error sources are shown in the figure. Steady state errors can be adjusted out with a potentiometer or DAC, but drift errors always must be accounted for because determine the minimum output voltage. Notice that error sources are referred to the input so they have to be multiplied by the circuit gain to refer them to the output. Drift errors come in two categories: dc errors that change with time or temperature like bias current, or ac errors like power supply noise. A prudent design considers all error sources, eliminates some, and minimizes the remainder.

Signal-To-Noise Ratio

$$SNR = 20Log_{10}\left(\frac{V_{SIGNAL}}{V_{NOISE}}\right)$$

Data Converter Example:

$$LSB = \frac{FSV}{2^N} = \frac{3V}{2^{16}} = \frac{3V}{65536} = 45.8\mu V$$

$$V_{PS(INPUT)} = \frac{V_{PS}}{k_{SVR}} = \frac{10mV}{1000} = 10\mu V$$

Power supply noise cannot be ignored.

2-59

The system specifications and application determine the signal strength in most low voltage systems. System generated noise is usually lower because switched currents are lower, so the op amp noise becomes s significant contributor to the overall S/N ratio. Thus, the numerator of the signal-to-noise equation stays constant, and the denominator must decrease to get a higher S/N ratio.

In a 12 bit system the full scale output of a transducer may be 10mV, and this value translates into a least significant bit of 2.44μV. Given a power supply rejection ratio of 60dB 10mV of power line noise becomes 10μV. It is easy for the noise to overshadow the signal in low voltage systems.

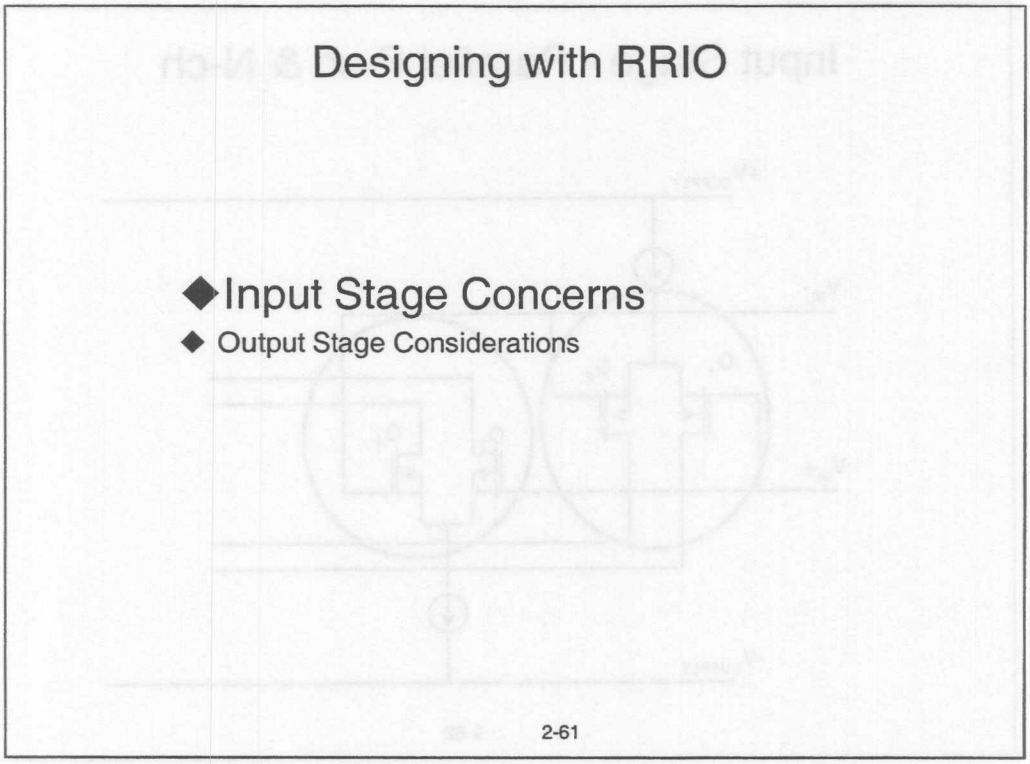
Comparing Op Amps

PARAMETER	LM324	TLV278X	TLV240X	UNITS	OPA340
V_{IO}	9	1.5	4.5	mV	0.5
ΔV_{IO}	No Spec	8	3	µV/°C	2.5
I_{IB}	500,000	100	350	pA	10
I_{IO}	50,000	100	300	pA	10
CMRR	50	50	65	dB	92
k_{svr}	65	70	100	dB	78 db
v_n	No Spec	18 (1 kHz)	500 (100 Hz)	$nV/(Hz)^{1/2}$	25nV @ 1k
I_n	No Spec	0.9 (1 kHz)	8 (100 Hz)	$fA/(rtHz)^{1/2}$	3

2-60

This chart compares three op amps. The LM324 is the first single supply op amp, and it is still one of the highest volume selling op amps. The input offset drift, noise voltage, and noise current are not specified, so this op amp, regardless of its low cost, is not used in challenging designs.

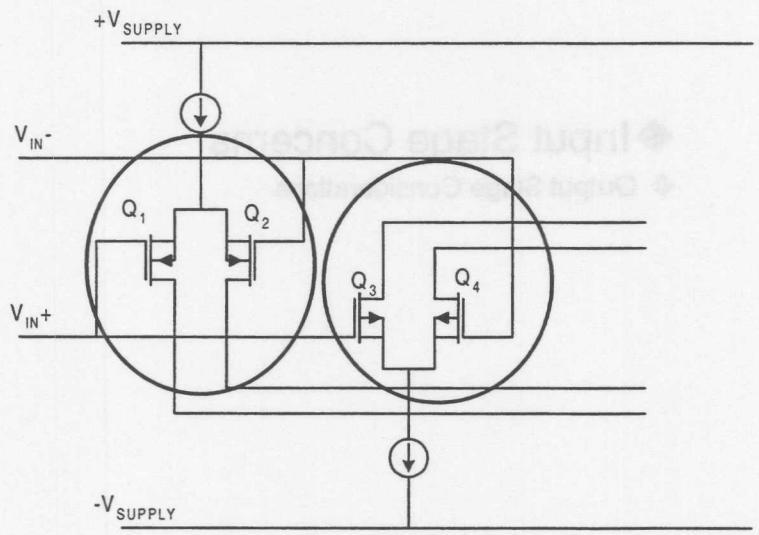
The TLV278X and TLV240X op amps are both recent designs aimed at low voltage applications. There are slight differences in the specifications because the bandwidths are so different. As usual, the low frequency op amp has the better specifications. Notice that all of the new op amp specifications are equal to or better than the LM324 specifications. This is why there is a trend away from the LM324 to new op amps.



The points made in this section apply to almost all of the rail-to-rail input and output op amps available. All devices are designed and built with similar topology and therefore they all respond in a similar manner. There is nothing here that is unique to any one manufacturer.

The circuit designer must also be aware of the nature of the device being used. It may not be necessary to have one of the rail-to-rail characteristics but that operation comes with the device chosen for other parameters and still must be dealt with.

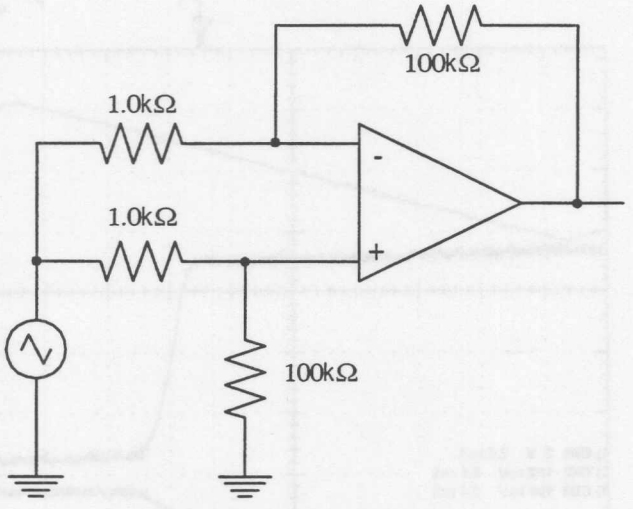
Input Stage - Parallel P-ch & N-ch



2-62

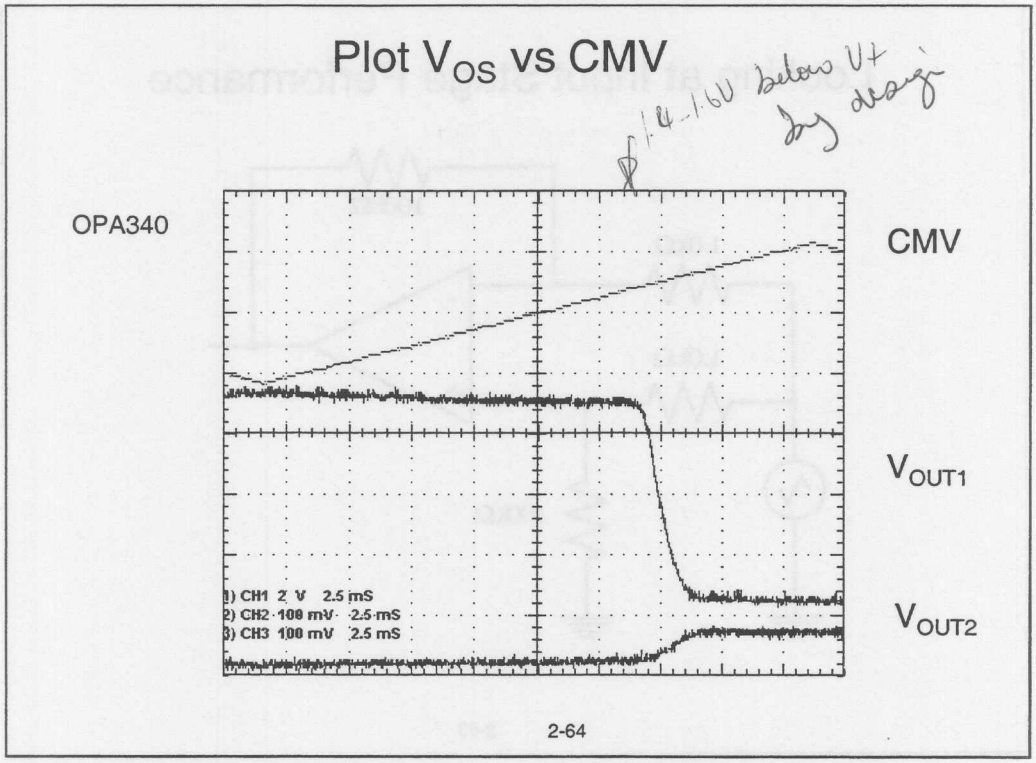
To accomplish rail-to-rail input conventional designs use two input stages, one P-channel and one N-channel. For common mode voltages near the positive rail the Q_3 and Q_4 are functional while Q_1 and Q_2 are turned off. Near the negative rail the opposite is true. There is a transition zone where both stages are on.

Looking at Input Stage Performance



2-63

To observe this change of control the differential gain of 100 circuit is built. Apply a triangle wave shape as a common mode voltage and observe the output.



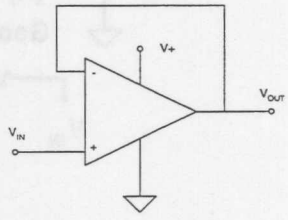
The top trace is the input signal swinging from -2.5V to +2.5V. The middle trace is the output of one OPA340 and the bottom trace is the output of the second OPA340 in the same package. The

Performance Requirements

The simple buffer stage.

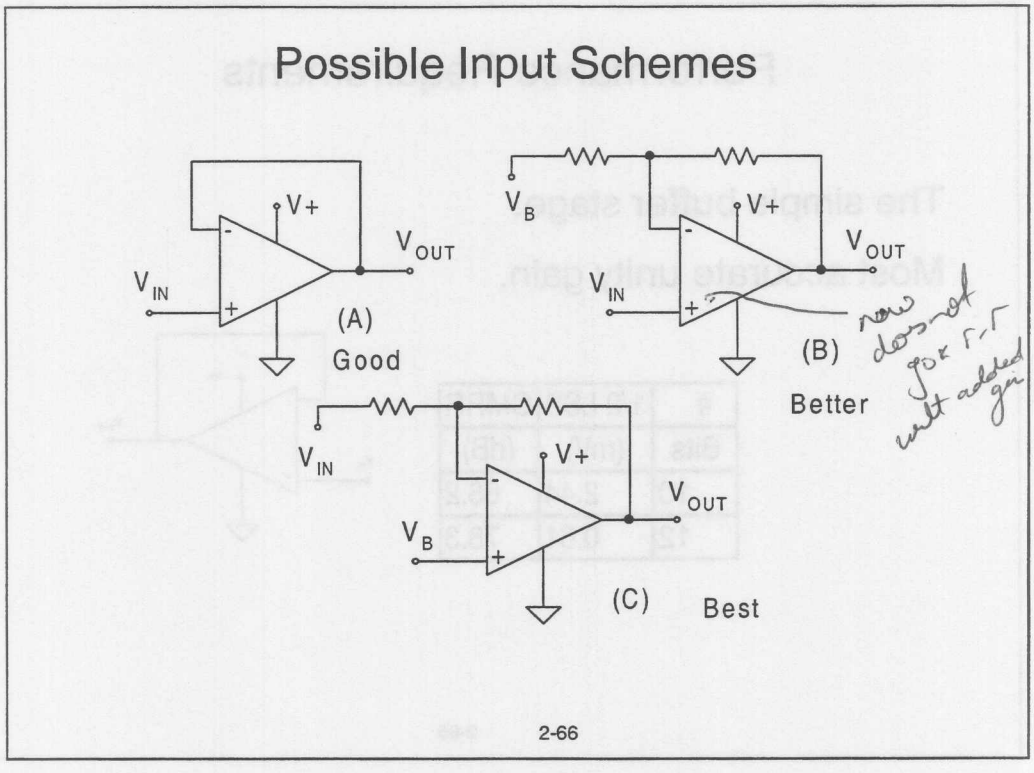
Most accurate unity gain.

# Bits	1/2 LSB (mV)	CMRR (dB)
10	2.44	66.2
12	0.61	78.3



2-65

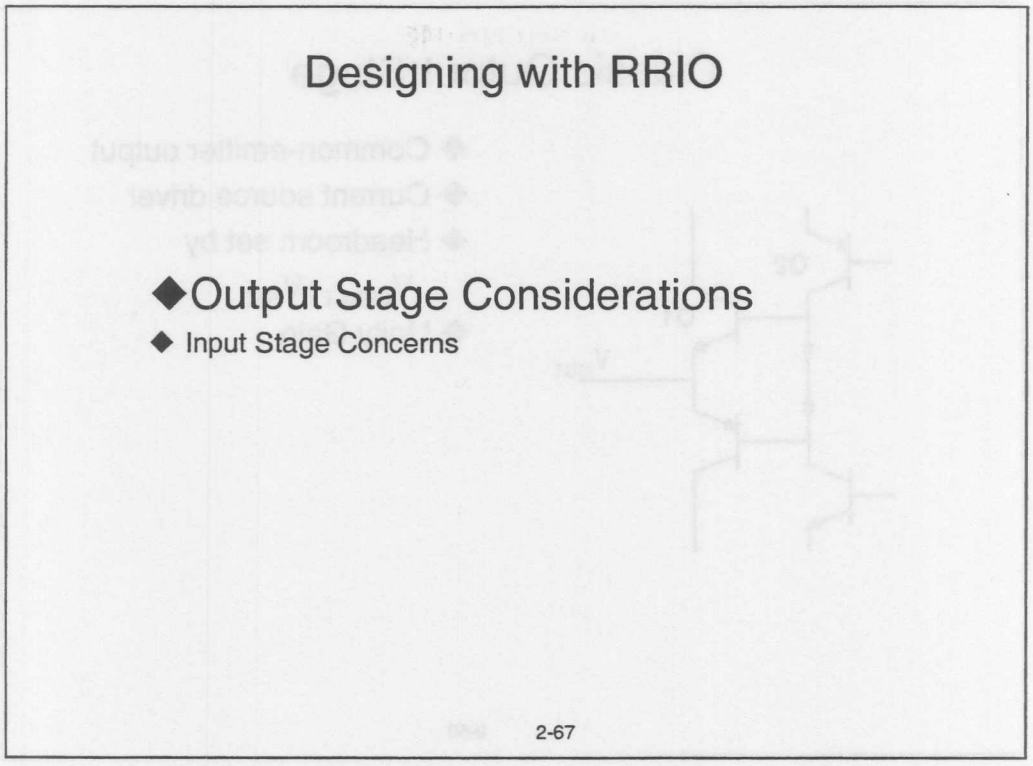
The unity gain buffer has the greatest gain accuracy but is the most demanding for common-mode rejection ratio (CMRR). The chart lists the required common mode rejection ratio for the various ADC resolutions. This is for the CMRR over the full input range.



Circuit A. This has been discussed. Shown here for completeness.

Circuit B. To avoid the CMV transition region it is possible to operate the op amp in a gain about a bias point established at V_B. At least one family of rail-to-rail input op amps have the transition region at about 1.5 to 1.7V below the positive rail. If the op amp is operated on 3.3V supplies and the V_B set at a voltage midway between the rails the operating point could end up in the transition zone.

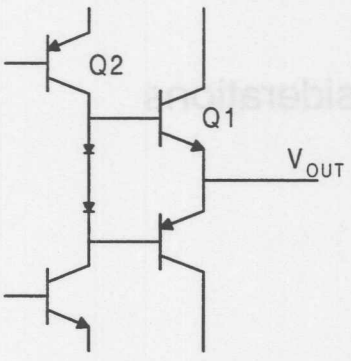
Circuit C. The best possible solution could be to operate the op amp in an inverting configuration with bias. In this mode the common mode signal never moves so there can not be any distortion.



The rail-to-rail output stages can have hidden impact on a design.

Classic Output Stage

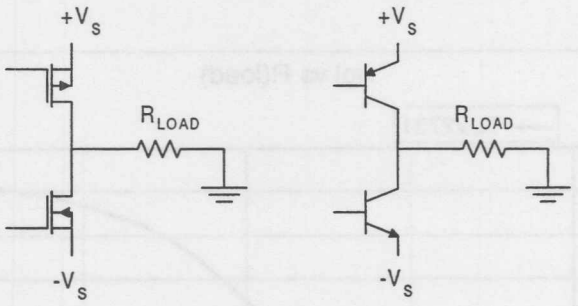
- Common-emitter output
- Current source driver
- Headroom set by $V_{CESAT}+V_{BE}$
- Unity Gain



2-68

Classic output stages have excessive headroom requirements because of the circuit topology. Two transistors and associated bias circuitry will push the headroom drop to over 2V.

R-to-R Output Stage

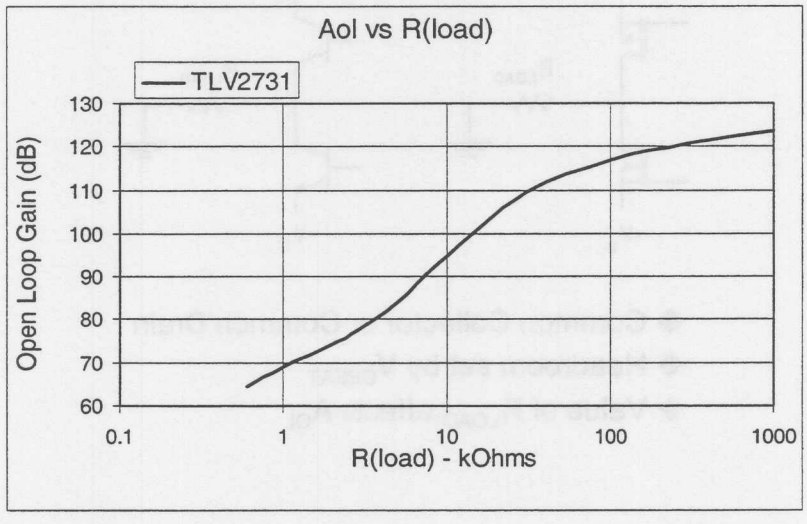


- Common Collector or Common Drain
- Headroom set by V_{CESAT}
- Value of R_{LOAD} affects A_{OL}

2-69

Rail-to-rail output stages reduce the headroom requirement to very low values, however there is a price. This condition happens in both FET and bi-polar transistor devices. The output stage is now a gain stage. To visualize this look at the NPN device in the circuit on the right side. The gain of that stage is $R_{LOAD}/R_{emitter.}$ At a minimum the emitter resistor of that stage is the bulk emitter resistance of the transistor.

A_{OL} as a function of R_{LOAD}



2-70

This shows the typical relationship between open loop gain and R_{load}. Working with a single 5V supply a 10k load resistance would not be unreasonable. The part should be able to supply the 1/2mA requirement associated with that load resistance.

Circuit Equations

Inverting Stage

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_I}\left(\frac{1}{1+\frac{R_I+R_F}{R_I A_{OL}}}\right)$$

and

Non-Inverting Stage

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_I+R_F}{R_I}\left(\frac{1}{1+\frac{R_I+R_F}{R_I A_{OL}}}\right)$$

2-71

The gain equations that have been presented in other forms earlier show the affect of A_{ol} on the closed loop response.

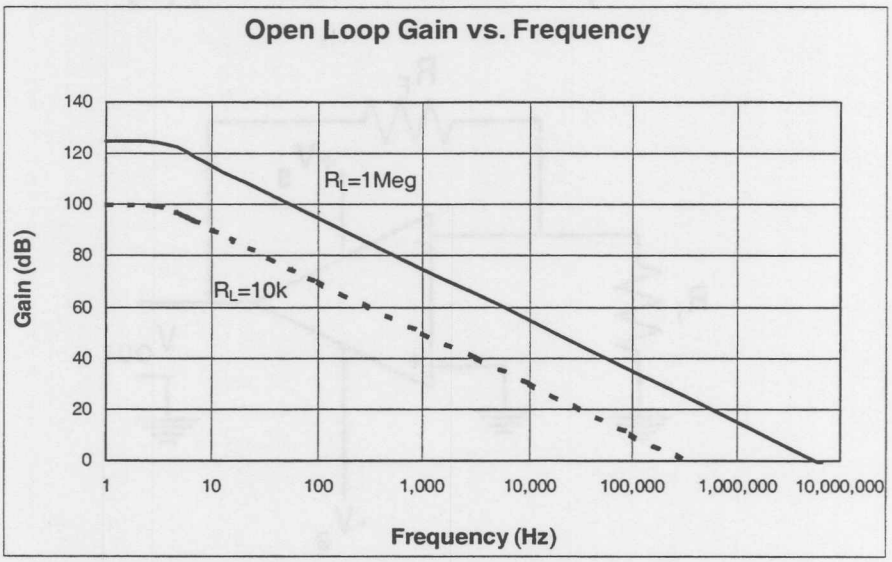
The Error This Can Cause

Open Loop Gain		Closed Loop Gain (V/V)			
Gain(dB)	Ratio(V/V)	1	10	100	1000
60	1,000	0.999000999	0.990099010	0.909090909	0.500000000
70	3,162	0.999683872	0.996847690	0.969346564	0.759746889
80	10,000	0.999900010	0.999000999	0.990099010	0.909090909
90	31,623	0.999968378	0.999683872	0.996847690	0.969346564
100	100,000	0.999990000	0.999900010	0.999000999	0.990099010
110	316,228	0.999996838	0.999968378	0.999683872	0.996847691
120	1,000,000	0.999999000	0.999990000	0.999900010	0.999000999

2-72

Actual gain calculation showing the result from giving up open loop gain.

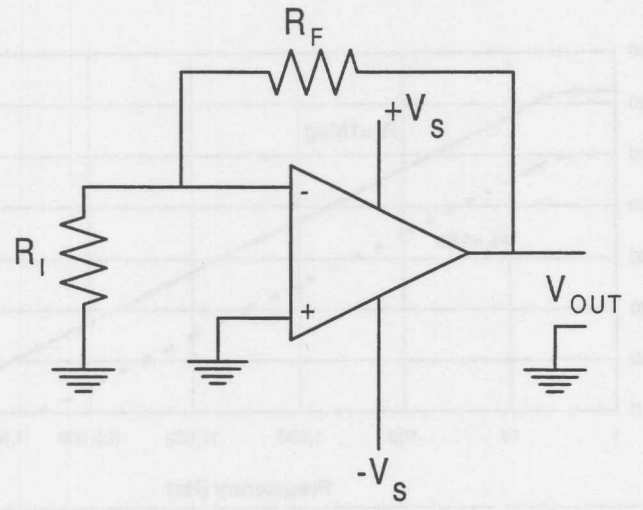
A_{OL} vs Frequency



2-73

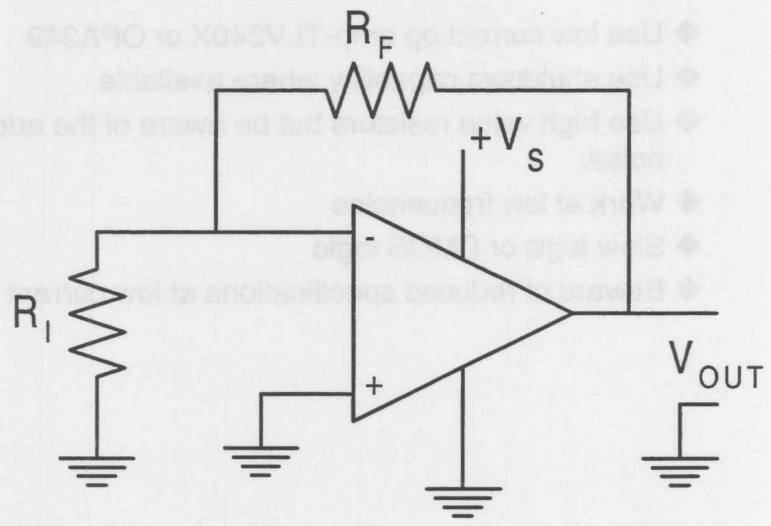
A 10k load resistance can reduce the useable bandwidth at unity gain from approximately 60kHz to 2kHz.

Output Offset - Dual Supply



Under dual supplies this circuit will demonstrate the op amps input voltage offset. The output voltage divided by the gain is the offset. This works because the perfect output zero point is the voltage at the non-inverting input.

Output Offset - Single Supply



2-75

In a single supply configuration, with ground as both the negative rail and the non-inverting input, the output cannot get to the required zero point. Measurements made with this circuit can appear that the op amp does not meet its offset voltage spec. The situation is more confused because changing the gain will not change the indicated offset voltage when it should.

The correction is to establish a signal ground that is midway between the supply rails. This will be the potential at the non-inverting input, the R_I return and the reference for the output voltage measurement.

Low Current

- Use low current op amp-TLV240X or OPA349
- Use shutdown capability where available
- Use high value resistors but be aware of the added noise.
- Work at low frequencies
- Slow logic or CMOS logic
- Beware of reduced specifications at low current

2-76

Points to consider when designing for low supply current draw.

Op Amp Selection Chart

Ultra Low Voltage (RRIO) (Supply Voltage <2.5V)

PART	Notes	S, D, Q	Vsup	GBW (MHz) Typ	Iq/Amp (mA) Max	OFFSET (mV) Max	DRIFT (uV/C) Typ	Ib (pA) Max	Vin Low Min	Vin High Max	Vout Low	Vout High	Vsup Spec	$$ in 1000s
Excellent Speed/Power Ratio														
TLV276*x*	SOT23, SD	S, D, Q	1.8 to 3.6	0.5	0.028	3.5	9	15	0	3.6	0.02	3.58	3.6	$ 0.55
OPAy347	SOT23	S, D, Q	2.3 to 5.5	0.35	0.034	6	2	10	-0.2	5.2	0.015	4.985	5	$ 0.46
nanoPower – POWER SAVERS!														
TLV240*x*	SOT23, Rev. Batt Prot.	S, D, Q	2.5 to 16	0.005	0.95μ	1.2	3	300	-0.1	10	0.15	4.95	+5	$ 0.75
OPAy349	SOT23	S, D	1.8 to 5.5	0.07	2μ	10	10	10	-0.2	5.2	0.3	4.7	+5	$ 0.69
TLV224*x*	SOT23	S, D, Q	2.5 to 12	0.005	1.5μ	3.5	3	300	-0.1	10	0.15	4.95	+5	$ 0.55

y: Single=No Number, Dual=2, Quad=4
x: Single=1 (w/SD=0), Dual=2 (w/SD=3), Quad=4 (w/SD=5)

2-77

A brief selection of the many RRIO op amps available from TI.

A Common Problem

- Goal -- "Clean" ground for signal
- Problem -- Signal reference (Ground) is:
  - Very noisy
  - Changing
  - Not at ZERO volts

  OR
  - Ground loop current

2-78

The next topic is what could be called a "common problem." The issue is the need to have a signal referenced to a very clean ground so that it can be input to an A/D Converter. This signal may exist coming from a sensor which has a very noisy ground or a ground changing with time, or maybe a signal reference at a high voltage. In any case the ground is not what would be desirable to have as the reference potential for an A/D Converter. Another possibility is that connecting the two grounds, the ground from the sensor and the ground from the A/D converter, may cause a ground loop. That is a path for current flow within the grounding system. This current flow can cause a voltage drop that would give the signal an offset or a false signal that can't be tolerated.

SOLUTION ! ! !

Instrumentation Amplifier

(INA)

The LINEAR SUBTRACTOR

2-79

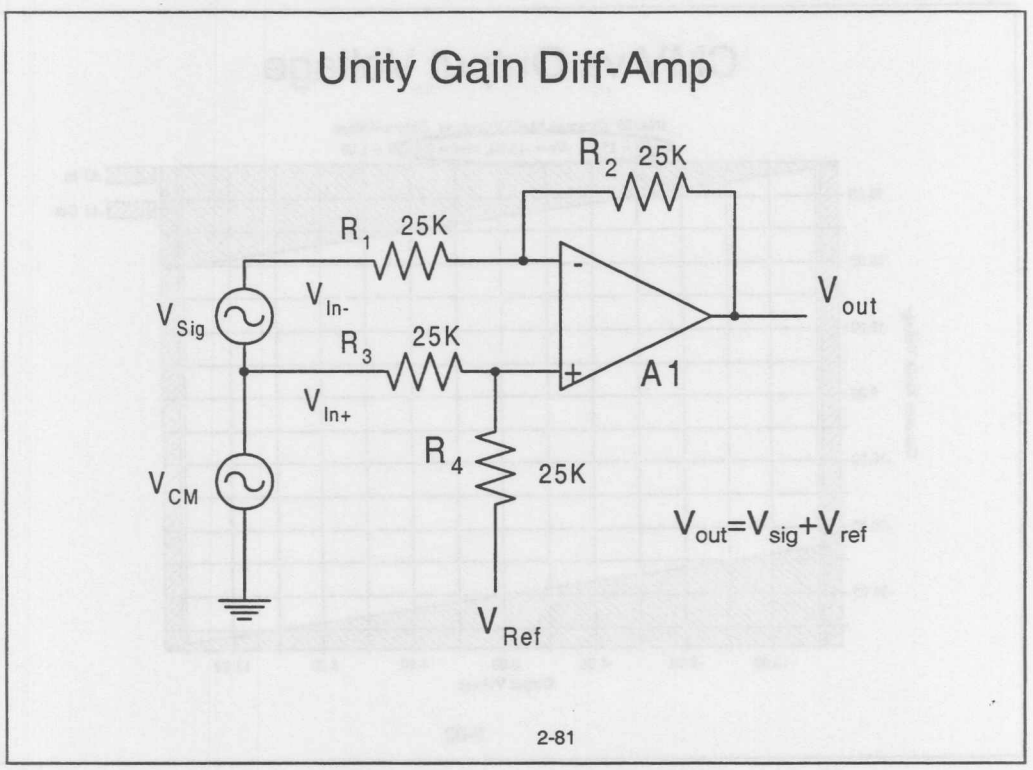
The solution is an "Instrumentation Amplifier": An instrumentation amplifier is simply a linear subtractor. A circuit that will take one signal and subtract it from another. It will take a sensor output signal and subtract it from its associated, noisy ground, giving a clean signal which can then be applied to an A/D converter. With an instrumentation amplifier signals cannot be added, non-linear functions are not possible, frequency dependent functions are not allowed. It simply subtracts one signal from another.

Instrumentation Amplifiers

- Features:
  - Superior common mode noise rejection
  - Differential Inputs
  - Gain setting via a single resistor(usually)
- There are specific INAs for:
  - Single Supply Applications
  - Low Noise Applications
  - Very High Impedance Sources

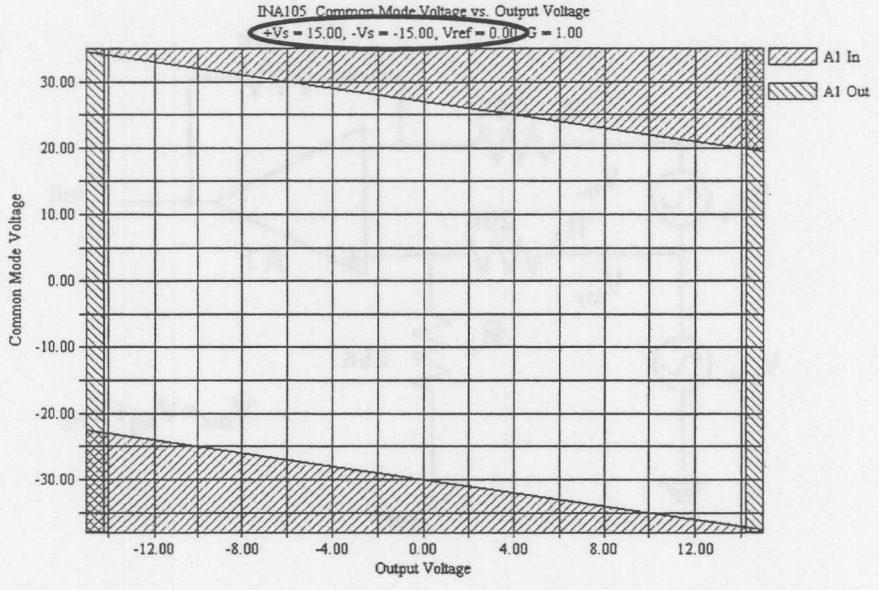
2-80

To do this instrumentation amplifiers provide superior common mode noise rejection using differential inputs. The gain is usually set with a single resistor. We have developed a couple of exceptions for that now. There are specific INA's for single supply operation, low noise, very high common mode voltage and very high output impedance sensors.



The difference (diff) amp is the simplest instrumentation amplifier or linear subtractor. A diff amp is a an op amp with precision resistors that are laser trimmed at the wafer level such that the ratio of R_1 to R_2 is the same as R_3 to R_4. Notice the ratio is trimmed not the absolute value of these resistors. This will become very significant in future circuits. Shown here is a differential signal between the inputs, this is offset by a common mode voltage. The common mode voltage could be noisy or could be of high value. It could be changing with time or it could be a DC level as would be output from a bridge circuit. It has a differential input signal single and a single ended out put signal which is referred to the Vref pin. For this unity gain diff anp the output then is equal to $V_{in}+V_{ref}$. The value of V_{ref} is typically midway between supplies but it not be. In a normal application the V_{ref} pin would be tied directly to the analog ground pin of the A/D Converter. This gives the best condition for the signal to be applied to the A/D Converter.

CMV vs Output Voltage

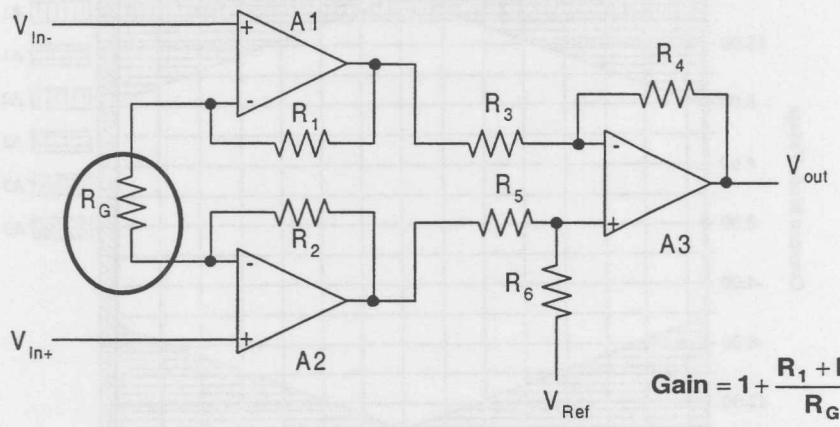


2-82

The allowed common mode voltage is shown here as a function of output voltage. As the output voltage becomes more positive, the allowed common mode voltage approaches -35 volts. As the output goes negative, the allowed common mode voltage goes beyond +30 volts.

Download software from web.

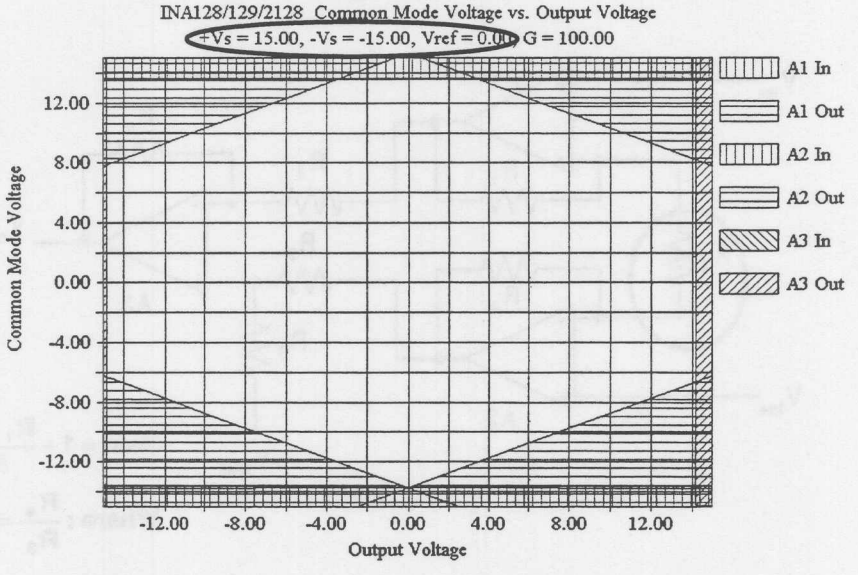
Instrumentation Amplifier - 3 Op-Amp Topology



2-83

The classic instrumentation amplifier is the 3 op amp INA shown here. The 3 op amp INA has the familiar diff amp as the output stage with added input buffers. The input stage provides a high input impedance as well as the ability to amplify the input signal. It's the network at A3 with resistor ratio trimming that sets the common mode rejection of this circuit. The gain set resistor (R_G) is generally supplied by the user. To assure the accuracy of the gain equation the values of R_1 and R_2 are trimmed for absolute value.

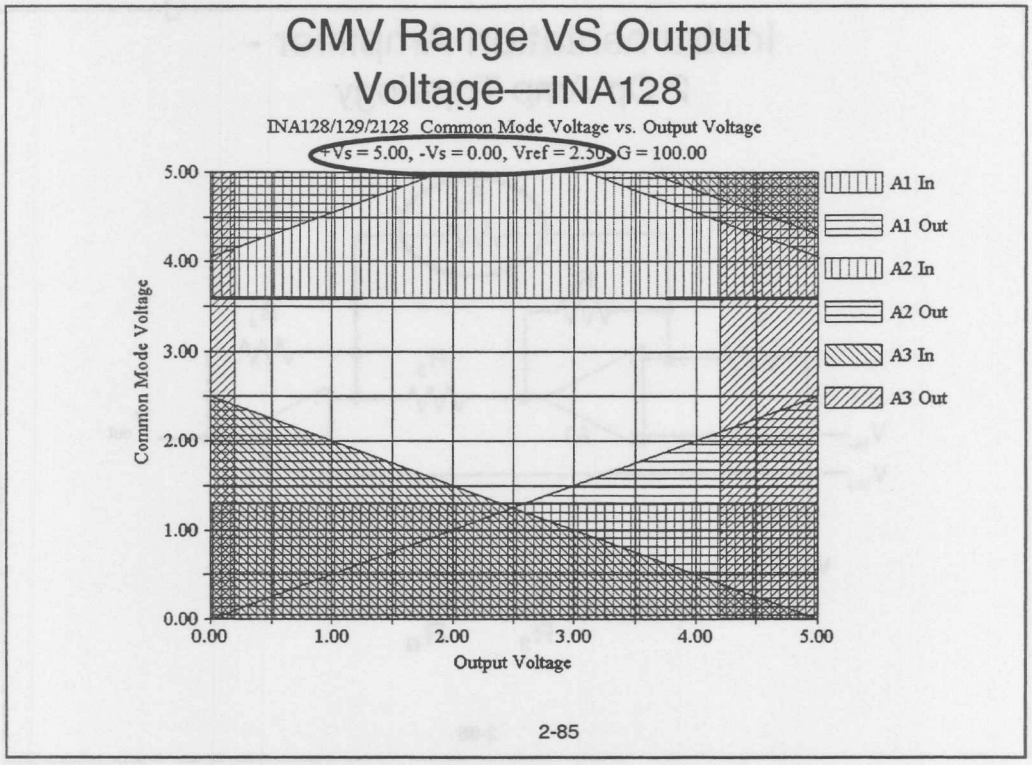
CMV Range VS Output Voltage—INA128



2-84

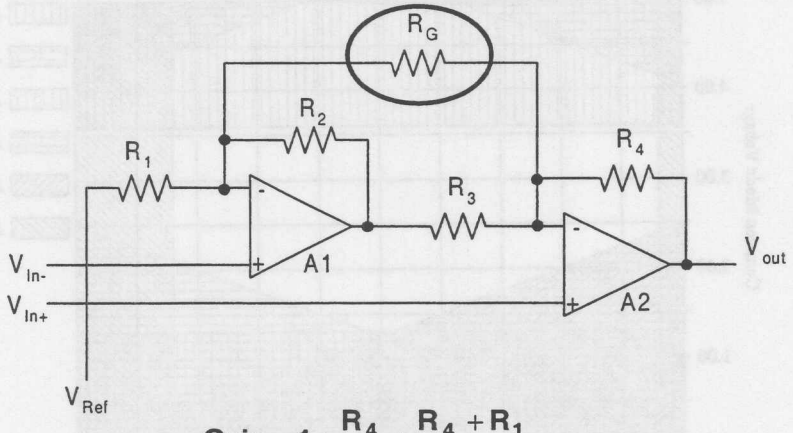
This is a plot of the allowed common-mode voltage verses output voltage for the INA128. This is a classical 3 op amp INA. At low output voltage there is a very wide common mode voltage range. As the output voltage increases the allowed common mode voltage range decreases.

Download SW from Web



This is the same plot when operating with a single 5V supply, and with the reference at the mid-point of the supply rails. The window of allowed common mode voltage closes considerably. The common mode rejection is still functional if the common mode voltage can be kept within these limits.

Instrumentation Amplifier - 2 Op-Amp Topology



$$\text{Gain} = 1 + \frac{R_4}{R_3} + \frac{R_4 + R_1}{R_G}$$

2-86

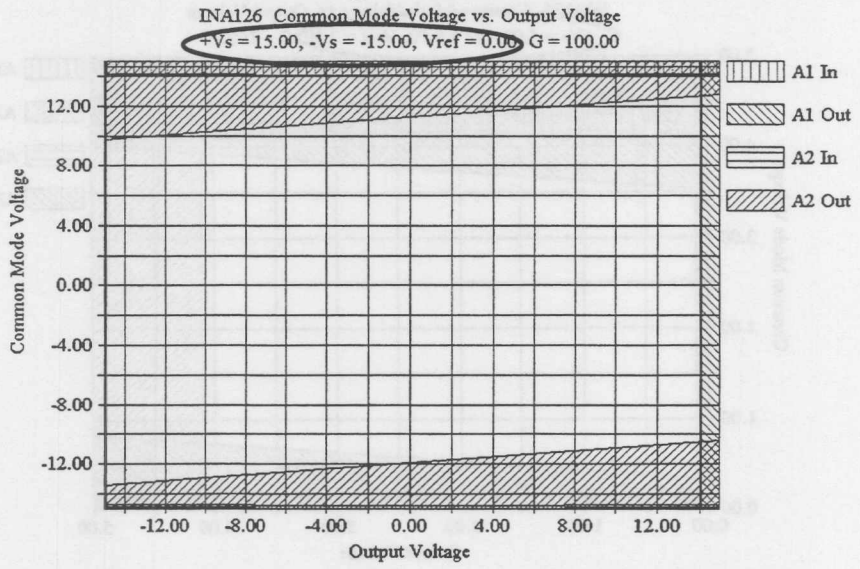
This is the 2 op amp topology INA with the single gain-set resistor shown here as R_G. It has advantages in that it uses one less op amp. Therefore, the die will be smaller which implies a lower cost and it is going to draw lower quiescent current.

One draw back is that the gain must be greater than one. For the INA126, because of the resistor values of 10k and 40k for R_1 and R_4, the gain equation is .

$$\text{Gain} = 5 + \frac{80k}{R_G}$$

Another drawback with this circuit is that the common mode rejection falls off with increased frequency a little faster than the 3 op amp INA. This happens because the plus input is applied directly to the output op amp while the minus input must go through a preliminary stage before it is applied to the output op amp. The signal coming from the minus input is delayed which causes a phase shift. This phase shift will degrade the common mode rejection at higher frequencies.

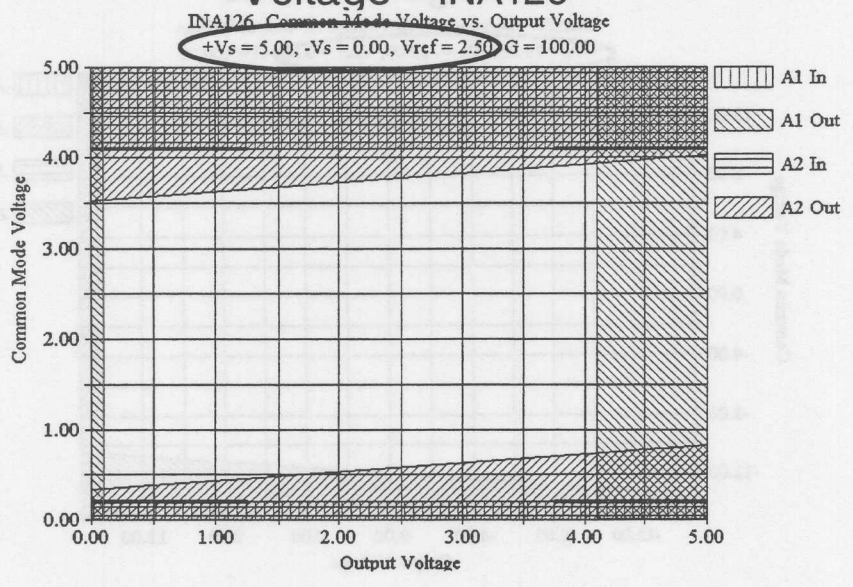
CMV Range VS Output Voltage—INA126



2-87

Another advantage is the significant improvement in allowed common mode voltage with increased output voltage. Operating from +/-15 V supplies with Vref at the midpoint the window of allowed common mode voltage has really opened.

CMV Range VS Output Voltage—INA126



2-88

Decreasing to a single 5V supply with the reference at midpoint still leaves a respectable window of allowed common mode voltage. It is possible that for a signal that requires a wide common mode voltage the 2 op amp INA maybe better advised in the circuit.

What is This Thing Called CMRR?

- A perfect subtractor:

$$V_{out}=A(V_{+IN}-V_{-IN})$$

- Real World Device:

$$V_{out}=A(V_{+IN}-V_{-IN}+\underbrace{K(V_{+IN}+V_{-IN})/2)}_{\text{Error Term}}$$

$$(V_{+IN}+V_{-IN})/2 = V_{CM}$$
$$(V_{+IN}-V_{-IN}) = V_{sig}$$

2-89

What is this thing called common mode rejection? For a perfect subtractor the output would be some gain constant, A, times the difference of the 2 inputs. That is the ideal world. In the real world, the output is the ideal term plus the error term. This term $(V_{+IN}+V_{-IN})/2$ is a way of expressing the common mode voltage.

CMRR Defined

The Real World Expression Becomes:

$V_{out}=A\ (V_{sig}+K\ V_{CM})$

Set: $V_{sig}=0$ and solve for K.

$K= V_{out}/\ (A\ V_{CM})$

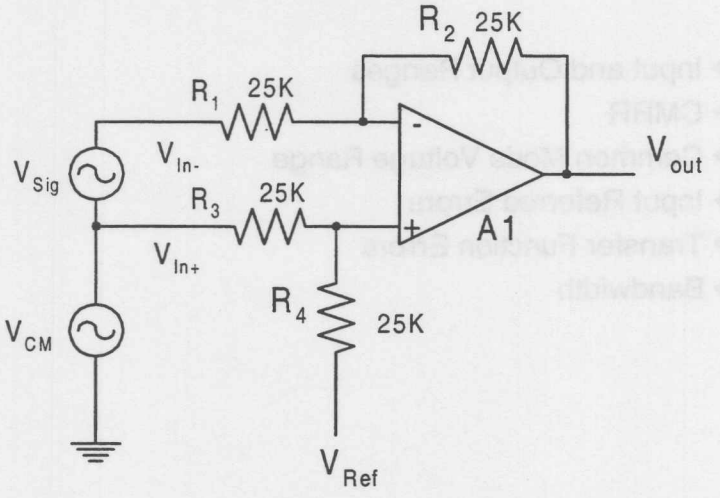
Which looks like a gain expression.

With units of μV/V or dB.

2-90

In the ideal world K would be zero. To determine K set the signal to 0 and then rearrange terms. The result looks like a gain expression V_{out}/AV_{CM}. This can be expressed in microvolts per volt or dB.

What This Parameter Means



2-91

To relate the CMRR to an actual amplifier set V_{sig}=0 and apply the maximum CMV.

Important specifications for Diff-Amps and INA's

- Input and Output Ranges
- CMRR
- Common Mode Voltage Range
- Input Referred Errors
- Transfer Function Errors
- Bandwidth

2-92

In addition to the common mode rejection and common mode voltage range errors or specifications to be concerned with instrumentation amps have input referred errors, transfer function errors and a limited bandwidth.

Input Referred Errors

- Voltage Offset (μV)

$$V_{OS} = \pm 50 \pm \frac{500}{G}$$

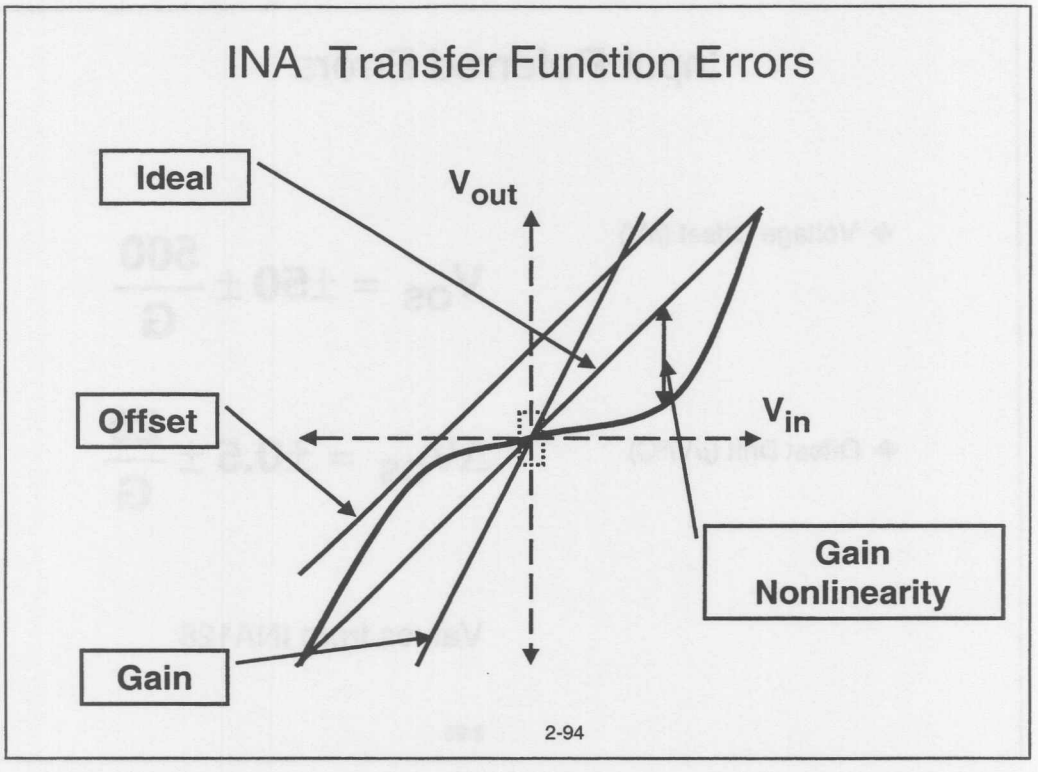
- Offset Drift (μV/ºC)

$$\Delta V_{OS} = \pm 0.5 \pm \frac{20}{G}$$

Values from INA128

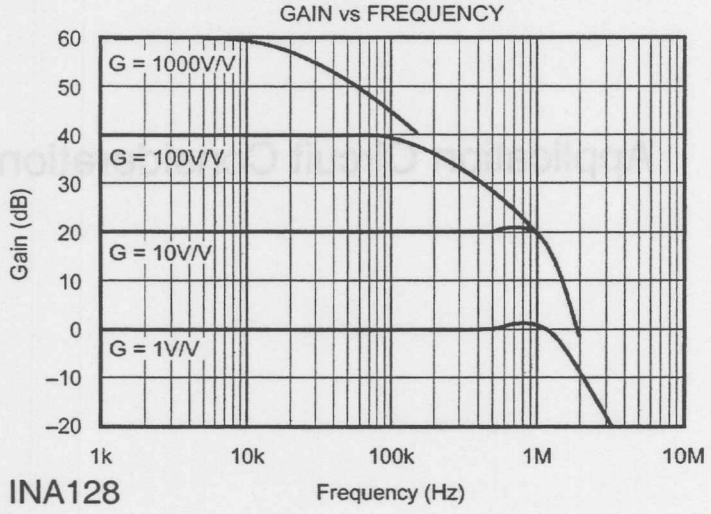
2-93

Input referred errors. The voltage offset from the specification table is composed of two components. The 50 μV in this case is related to the voltage offset of the input stage. The 500μV is the voltage offset of the output stage. This is the voltage offset as seen at the input. Multiply through by gain and the voltage offset RTI (Refer To Input) times the gain the output that would be 50 times the gain plus 500, 50 times the gain at a gain of one then would result in a maximum of 550 μV of offset. Operating at a gain of 10 then would result in 10 times 50 plus 500 or 1000 μV, 1mV of offset at the output as the gain goes up. Similar type relationship applies to the voltage output drift.



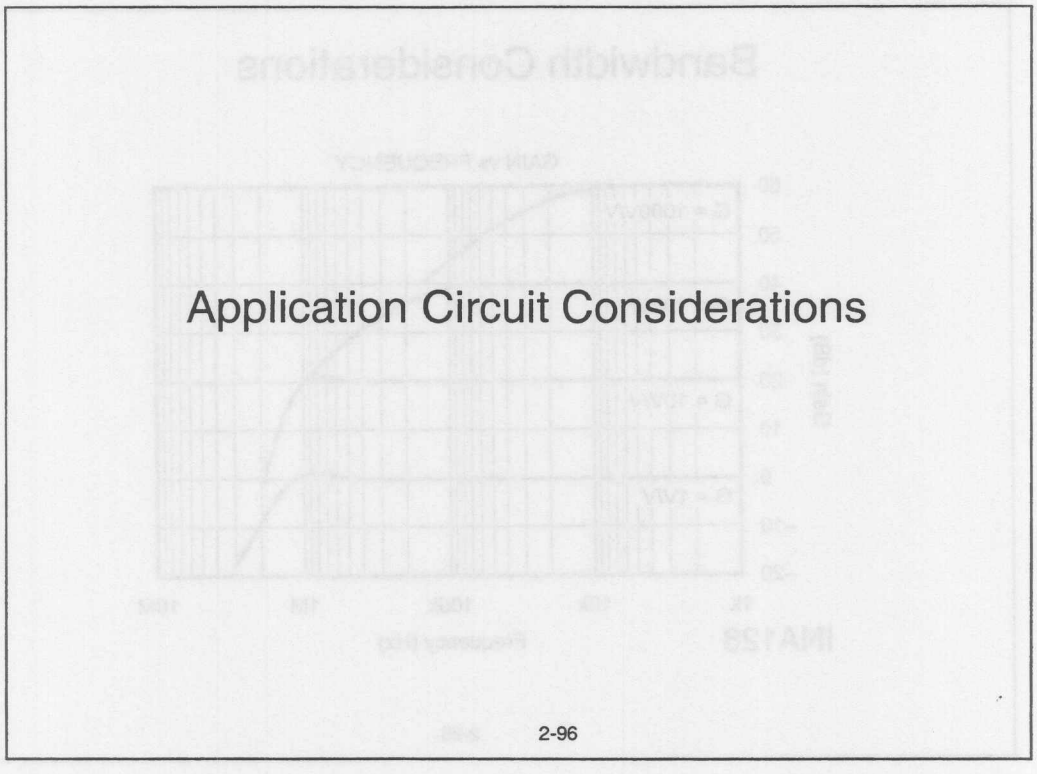
Transfer function errors are seen here. The ideal transfer function is the black line through the middle. A straight line that goes through the origin so that the transfer function is linear with zero error. Voltage offset is shown with the red line. Here it is a positive offset that will shift the linear transfer line up by the amount of the offset. A gain error would change the slope of the transfer line. It would still be passing through the origin but have a different slope. The final error is the gain non-linearity which is the maximum deviation from the ideal transfer curve after taking it to account voltage offset and gain error.

Bandwidth Considerations



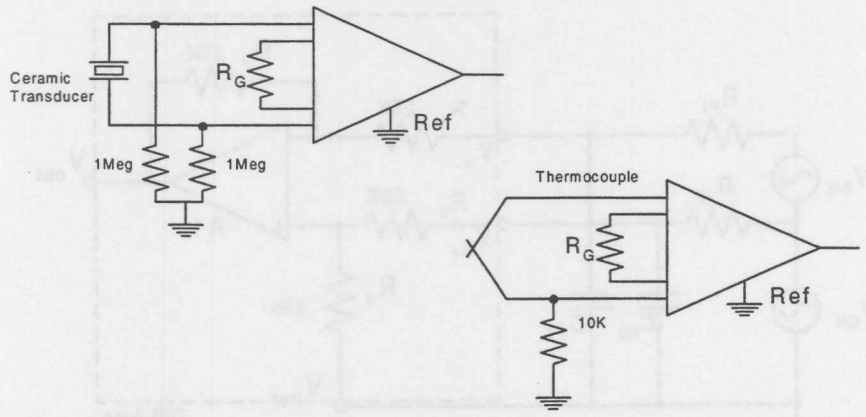
2-95

It is necessary to know the frequency response needed for the signals to be processed. It is not uncommon to see peaking in the lower gains from these instrumentation amplifiers. This is the frequency response of the INA128. It uses current feedback amplifiers in the front end which give a better frequency response.



For example there is a bias current associated with these amplifiers. Now they are some things looking at places to be concerned when you are designing the circuit and taking into account for your application.

Bias Current Path



2-97

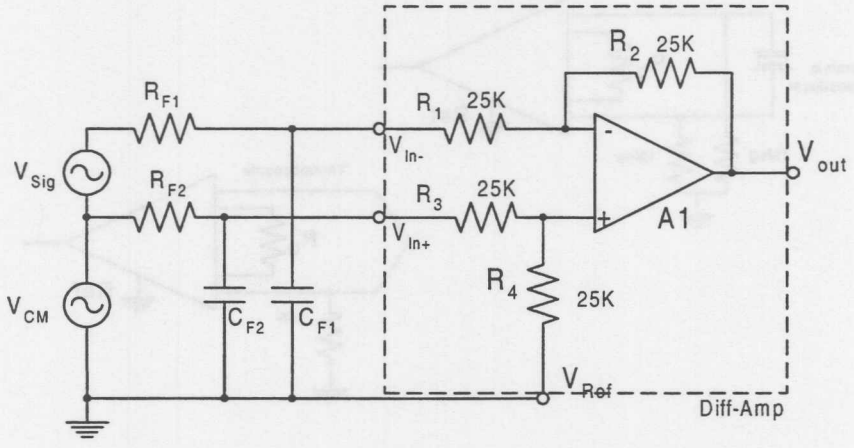
One concern that is often overlooked in instrumentation amplifier applications is the need to provide a path for bias current. The inputs are the non-inverting inputs of an op amp. This will demand some small bias current. This bias current path must be supplied by a resistive connection to either ground or one of the supply rails.

As a resistance to ground the resistor will form a voltage divider with the output resistance of the sensor. Therefore, its value should be as large as possible to minimize signal attenuation. From another point the bias current will flow through these resistors causing a DC offset. Therefore, the resistance should be as small as possible.

For example in the lower right is a thermocouple sensor application. The thermocouple will have a resistance of 10 to 20 ohms. A single resistor of 10K ohms will work well here. Since the thermocouple provides a DC current path through it, bias current can be supplied to both inputs with one 10k resistor.

In the upper left there is a ceramic transducer which will have an extremely high output impedance. A large resistor will be needed to supply the bias current without attenuating the signal too much. With the extreme high resistance of the ceramic transducer and no DC path through it two bias current resistors are needed.

Input Filters - Diff Amps

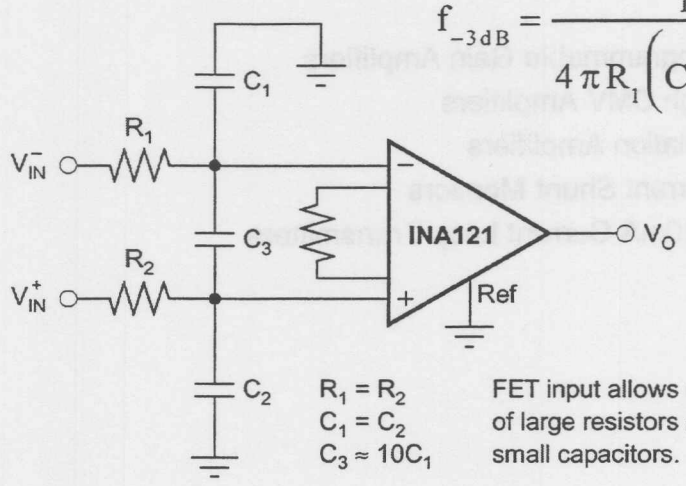


2-98

One thing that is attempted quite often is to add filtering in the input of an instrumentation amplifier. With a diff amp circuit like this it is generally invitation to disaster. The problem here is that the 25K resistors, while they are adjust laser trim at the wafer level for ratio match the absolute value is not controlled and can vary as much as 30%. If a perfectly balanced filter at the front end $R_{F1} = R_{F2}$ and $C_{F1} = C_{F2}$ is applied it still could upset the ratio. In addition the gain accuracy is disturbed. Therefore input filters on diff amps are a very poor circuit design.

Input Filters - INAs

$$f_{-3dB} = \frac{1}{4\pi R_1\left(C_3 + \frac{C_1}{2}\right)}$$



$R_1 = R_2$
$C_1 = C_2$
$C_3 \approx 10C_1$

FET input allows use of large resistors and small capacitors.

2-99

On a full instrumentation amp with very high input in impedance the situation is not quite as delicate. It is necessary for R_1 to equal R_2 as well as C_1 equal C_2. These filters reduce common mode noise. If the poles are not balanced then any difference will create a differential signal which will be amplified. The combination of R_1, R_2 with C_3 directly reduce the differential noise. A general rule is to choose C_3 equal to ten times the value of C_1.

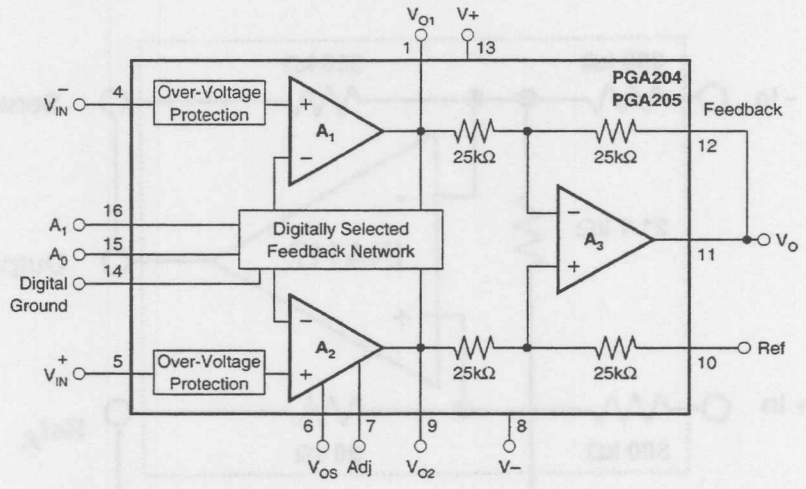
"Special" Instrumentation Amplifiers

- Programmable Gain Amplifiers
- High CMV Amplifiers
- Isolation Amplifiers
- Current Shunt Monitors
- 4-20mA Current Loop Transmitters

2-100

Within the broad span of instrumentation amplifiers there are several devices that have been developed to address unique situations.

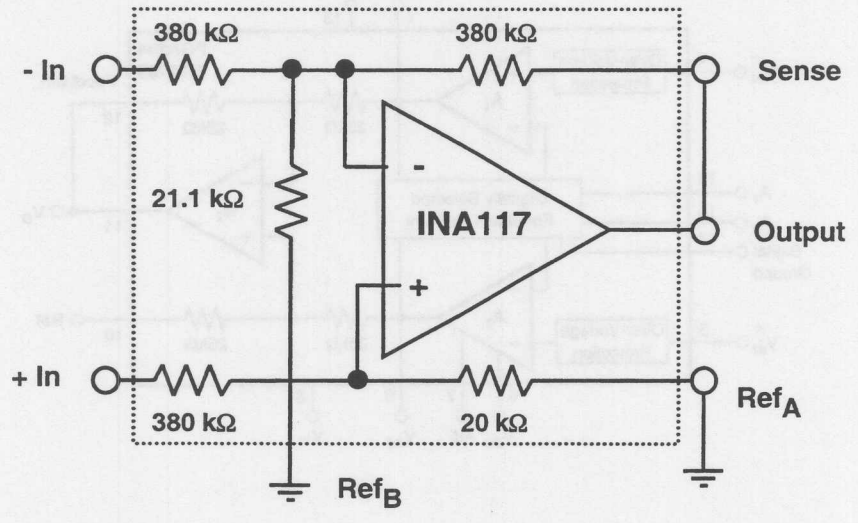
Programmable Gain Amplifier —PGA



2-101

Take a three op amp INA and add three gain setting resistors, a multiplexer with drive logic and the result is an INA that can have its gain set by a microprocessor or other logic.

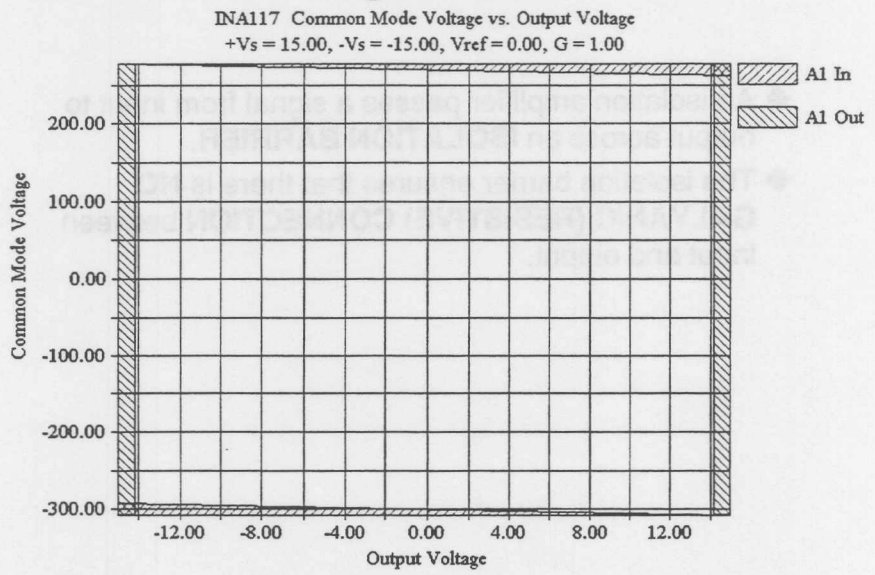
High CMV Diff - Amp, INA117



2-102

The allowed common mode voltage range of a diff amp can be greatly extended by the addition of one resistor. The INA117 is a direct example of this. The 21.1k resistor attenuates the input voltage and then sets a gain for the attenuated non-inverting input.

CMV Range VS Output Voltage—INA117



2-103

This is the CMV as a function of output voltage for the INA117. Notice that the window extends to near 300V.

What is An Isolation Amplifier?

- An isolation amplifier passes a signal from input to output across an **ISOLATION BARRIER**.
- The isolation barrier ensures that there is **NO GALVANIC (RESISTIVE) CONNECTION** between input and output.

2-104

In extreme cases where the common mode voltage can extend beyond the limits of the INA117 an isolation amplifier is needed. With an isolation amplifier there is no current flow between the input and the output.

Isolation Amplifiers

- Isolation Amplifiers are used to:
  - amplify and isolate low level signals in the presence of high common-mode voltages
  - Break ground loops and/or eliminate source ground connections
  - Provide an interface between patient monitoring equipment and ground.
  - Provide isolation protection to electronic instruments and equipment

2-105

Isolation amplifiers are used to break all galvanic paths between the input and the output. This may provide a safety barrier to protect a patient or a delicate piece of equipment.

Key Parameters

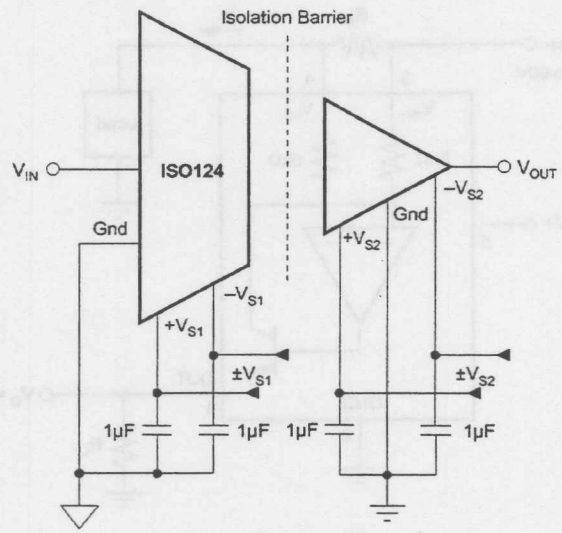
- Isolation Mode Rejection
  - Defined as the ratio of **differential signal gain** to the **isolation mode gain** at 60Hz. ISO122 has IMR of 140dB typ.
- Isolation Voltage Rating
  - Continuous rating specified at DC (e.g. 2121V for ISO102) and at 60Hz AC (e.g. 1500Vrms for ISO102)
- Gain Accuracy and Linearity

2-106

Isolation amplifiers add one more specification, IMR (Isolation Mode Rejection). For a large voltage across the isolation barrier measure the error that appears in the output signal. An IMR of 140dB is a rejection ratio of 10,000,000 to 1.

In addition isolation voltage, gain accuracy and gain linearity are of concern.

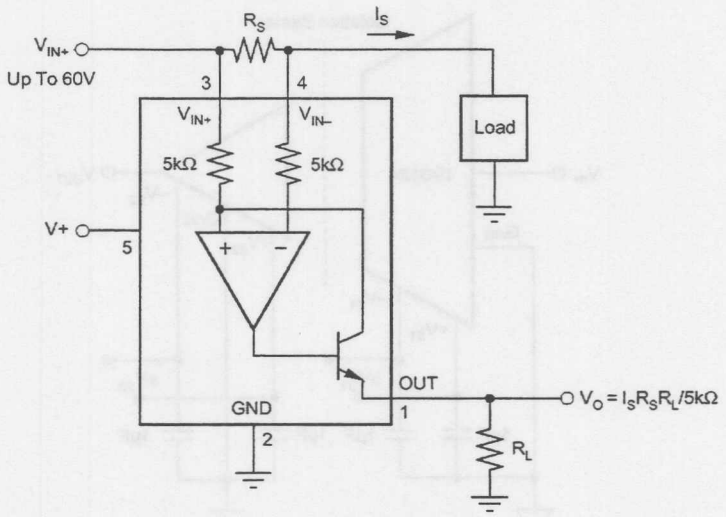
Isolation Amplifier



2-107

The ISO124 uses differential capacitors to transfer the information across the isolation barrier. It is necessary to furnish one power supply for the output stage and an isolated power supply for the input stage.

Shunt Current Monitor

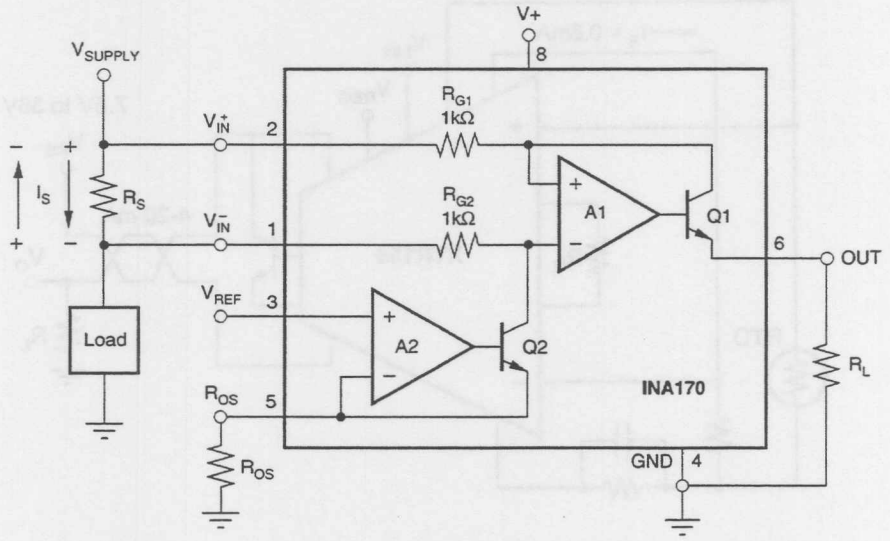


2-108

Another unique instrumentation amplifier is the shunt current monitor. With a user provided shunt resistor a voltage is developed through the 5k resistor at the V_{IN-} pin. The op amp turns on the transistor to draw current through the 5k resistor at the V_{IN+} pin such that the voltage across the input of the op amp is zero. Now the $I_S R_S$ voltage is equal to the $I_L R_L$ voltage which is V_O.

This circuit has several advantages. The die is very small so it fits in a SOT-5 package. The common mode voltage is independent of the supply voltage. The output signal is actually a current so it is possible to easily add or subtract signals.

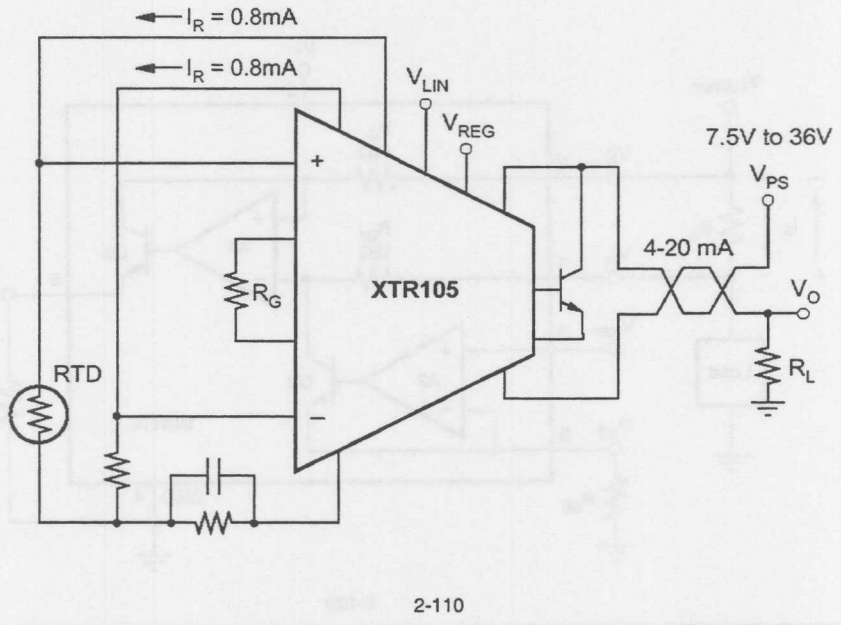
Bi-directional Shunt Current Monitor



2-109

The previous circuit will only work for current flow in one direction. This device develops an offset from ground so bi-polar current flow can be indicated relative to this offset potential.

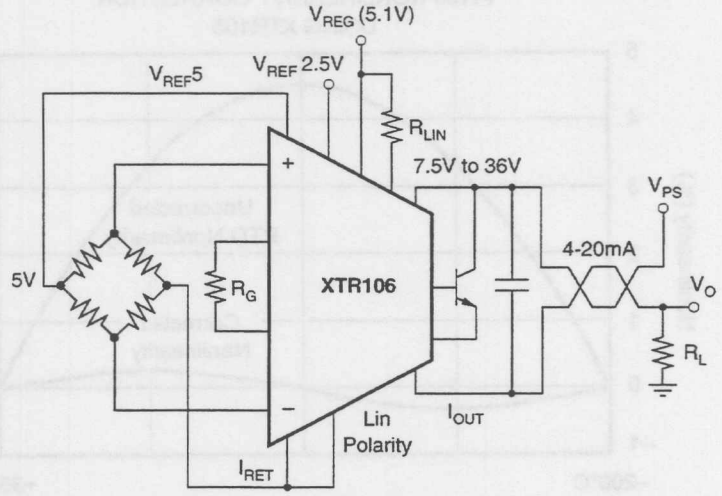
4-20mA Transmitters



2-110

This specialty instrumentation amplifier has several unique features. The input is differential with a limited common mode voltage range. Reference current sources are included to excite a 100Ω platinum RTD. The output is unique because the output signal is the current draw in the power supply line. With this system a sensor can be placed a great distance from a receiver and the only connection needed is a twisted pair of wires. Since the signal is the current in the wire voltage noise is rejected. Contact resistance and wire resistance are not a factor. The standard parameters are that a minimum reading is 4mA in the wire and the maximum is 20mA.

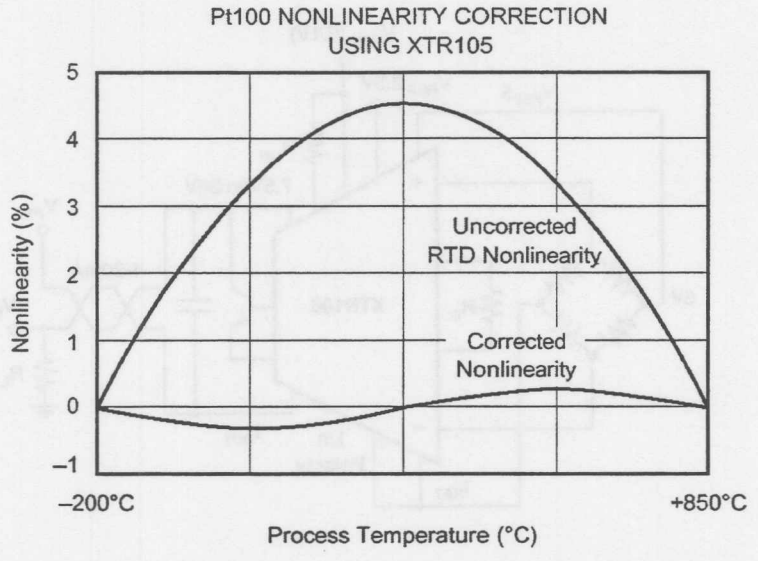
4-20mA Transmitters



2-111

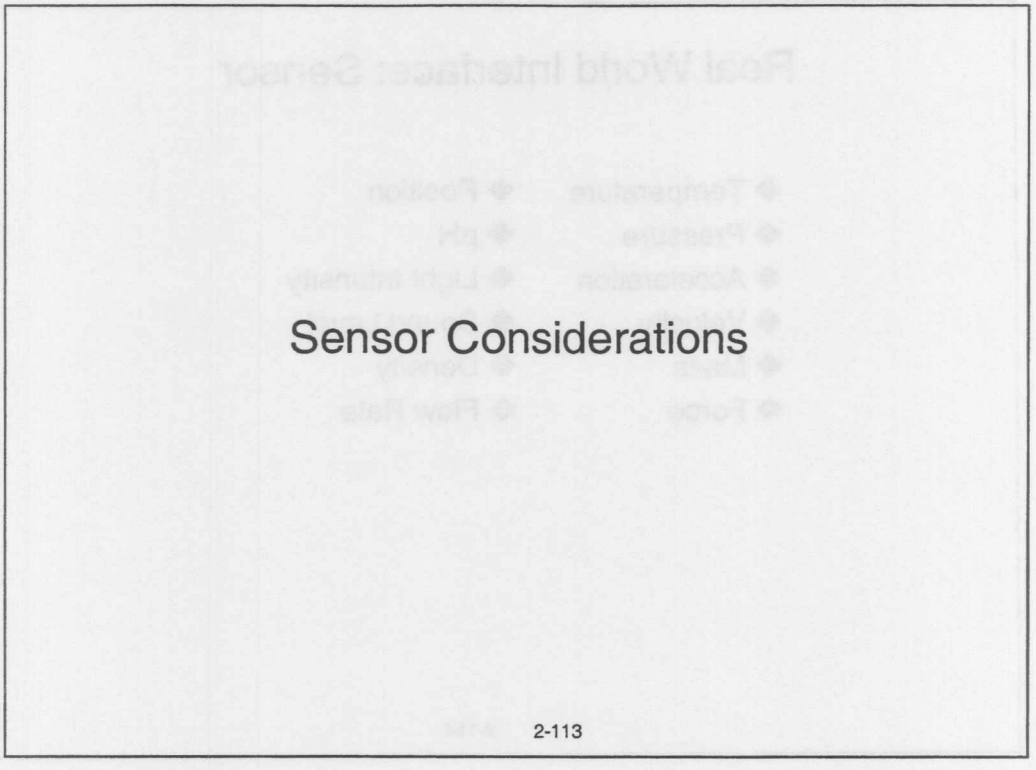
This is a different 4-20mA transmitter that is configured for bridge sensors. The reference source is a user selectable 2.5V or 5.0V voltage. An external transistor is suggested if not required to remove a major heat generator from the package.

Linearization Capability



2-112

Platinum RTDs are carefully crafted such that the resistance vs. temperature curve exactly fits a second order polynomial. Over the maximum temperature range of a RTD (-200°C to +800°C) the deviation from a straight line is about 4.5%. A circuit is included within most XTRs which will modify the reference source for the sensor to linearize the response. A quadratic nonlinear response is not unusual for some types of bridge sensors. The XTRs with a voltage reference on chip can be selected to correct for either positive or negative bow in the linearity curve.



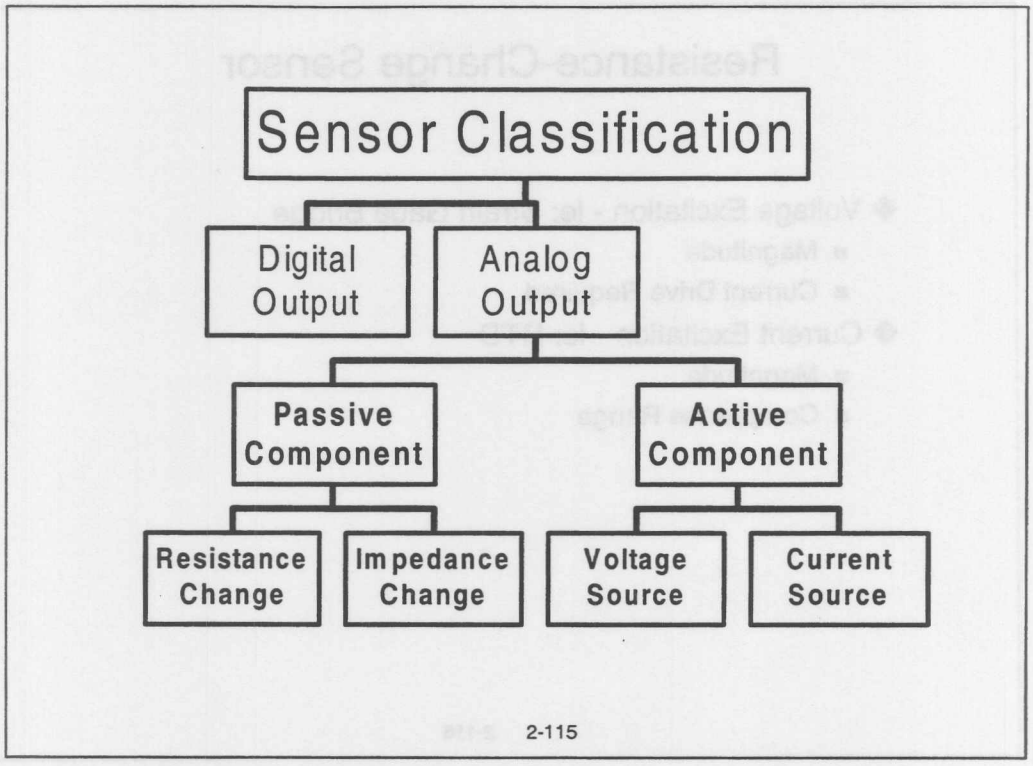
Sensors

Real World Interface: Sensor

- Temperature
- Pressure
- Acceleration
- Velocity
- Mass
- Force
- Position
- pH
- Light Intensity
- Sound Level
- Density
- Flow Rate

2-114

Physical properties that have devices for translation to electrical signals.



Classification of sensors. Passive component with proper excitation will transform to active sensor.

Resistance-Change Sensor

- Voltage Excitation - ie: Strain Gage Bridge
  - Magnitude
  - Current Drive Required
- Current Excitation - ie: RTD
  - Magnitude
  - Compliance Range

2-116

Those sensors that react to the physical parameter change with a change of resistance will need to have some form of excitation. Strain gage bridge structures are characterized with voltage excitation while RTDs are normally current source excited.

Voltage and Current References

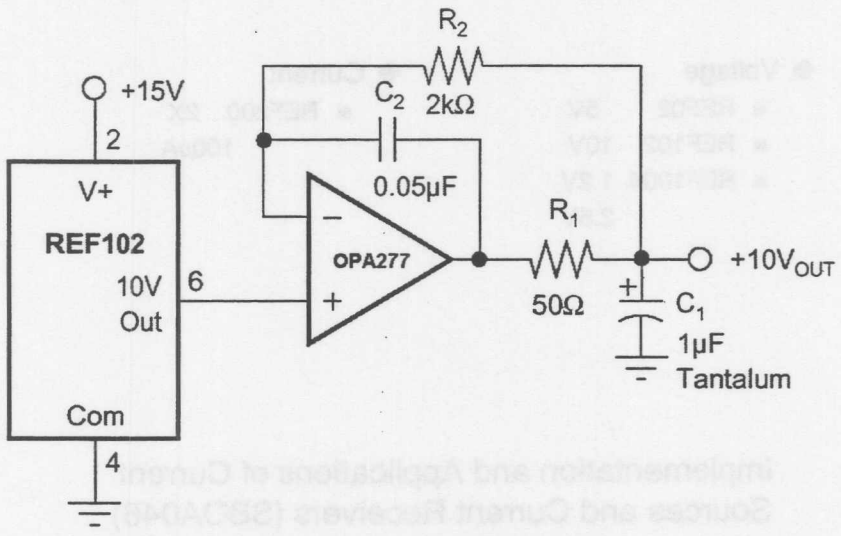
- Voltage
  - REF02 5V
  - REF102 10V
  - REF1004 1.2V
    2.5V
- Current
  - REF200 2X
    100μA

Implementation and Applications of Current Sources and Current Receivers (SBOA046)

2-117

References are available for both voltage and current sources. The application note on current sources contains good information on developing and using current sources and receivers.

Voltage Reference Filter



Voltage Reference Filters (SBVA002)

2-118

Some applications are sensitive to the noise associated with a voltage reference. This buffer/filter will help reduce the noise. Because the large capacitor can cause the op amp to oscillate it is usually necessary to add the stabilization network.

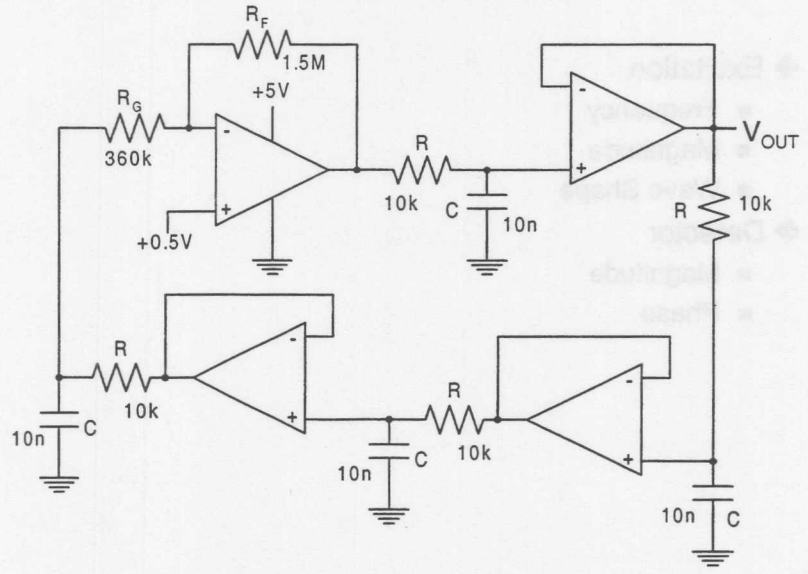
Impedance-Change Sensor

- Excitation
  - Frequency
  - Magnitude
  - Wave Shape
- Detector
  - Magnitude
  - Phase

2-119

There are sensors that work in an AC signal mode. Position may be indicated with a capacitance change on the micron scale. Large scale movement may be indicated with a Linear Variable Differential Transformer (LVDT).

The Bubba Oscillator
Sensor Excitation



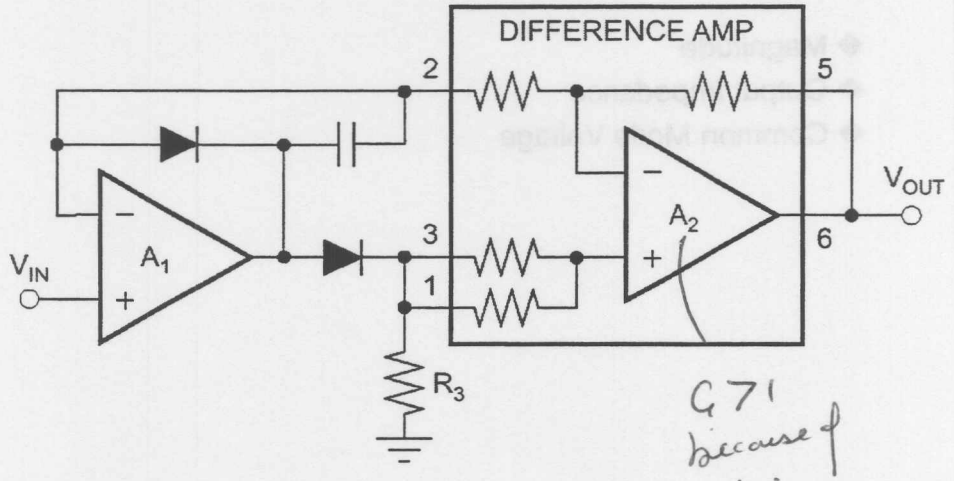
2-120

The phase shift oscillator accomplished in four stages of 45 degrees and one stage of 180 degrees. Each R-C pair is isolated from the next by the buffer op amp. Distortion is low and frequency stability is good. The cost is in the extra components Rs and Cs plus the fact that to change frequency requires changing four resistors and four capacitors.

More information on sine waves oscillators is available in the August 2000 issue of Analog Applications Journal (SLYT018)

PURE SINE WAVE

Absolute Value Circuit



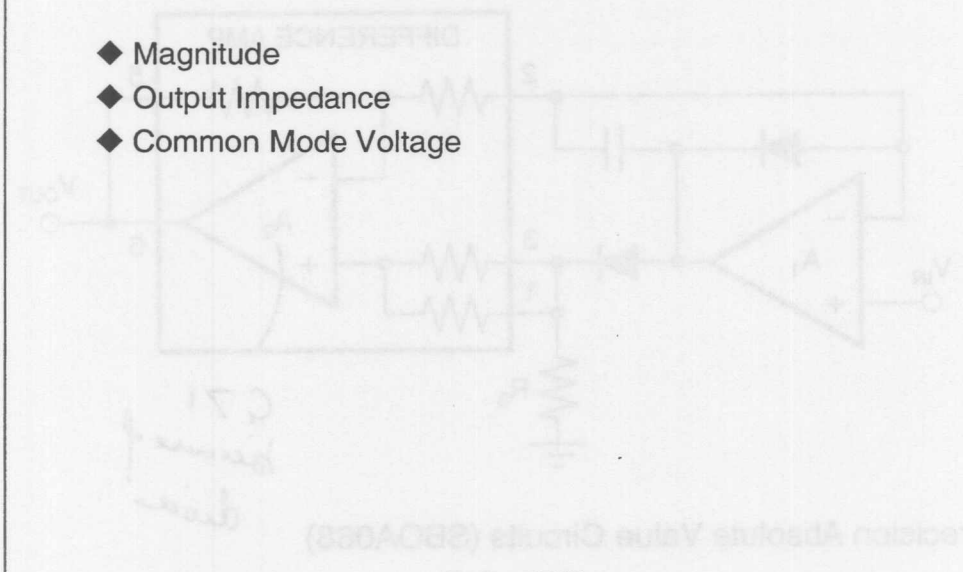
Precision Absolute Value Circuits (SBOA068)

2-121

The first stage in processing the signal from an AC sensor could be determining the absolute value of the waveform. This circuit, also called a precision rectifier, displays a gain of +1 for positive input signals and a gain of -1 for negative inputs. The accuracy of this circuit is dependent on the ratio of the gain to feedback resistors on the output stage. Using a diff amp with tightly controlled resistor ratios answers this problem.

Voltage-Source Sensor

- Magnitude
- Output Impedance
- Common Mode Voltage

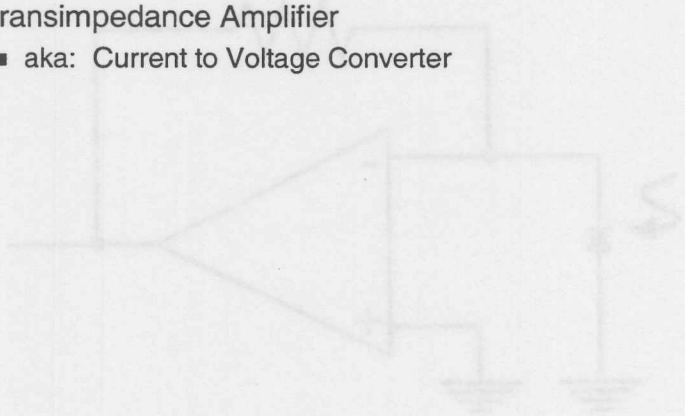


2-122

The significant considerations to interface with a voltage source sensor.

Current-Source Sensor

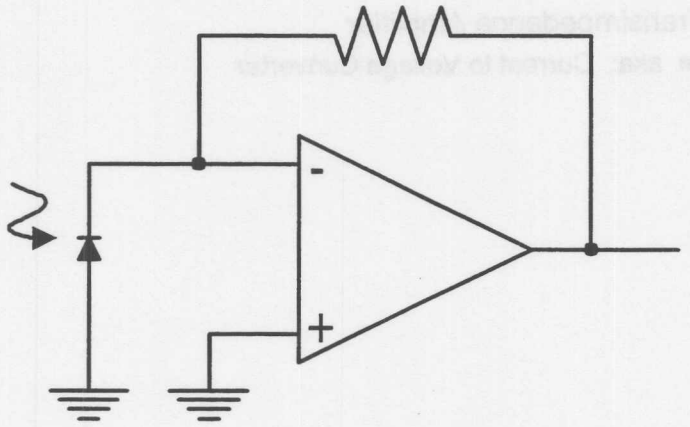
- Transimpedance Amplifier
  - aka: Current to Voltage Converter



2-123

There is a class of sensors that present a current change with change of physical parameter. The transimpedance amplifier is useful to convert this signal to a useable voltage.

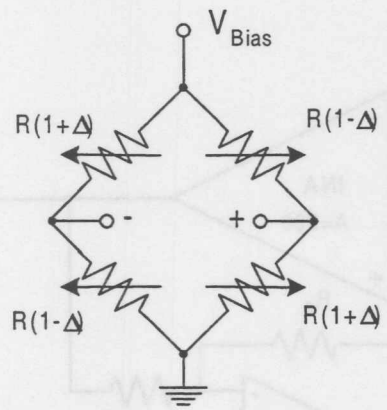
Transimpedance Amplifier



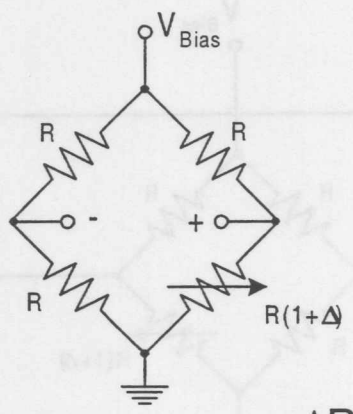
2-124

This application uses the operational amplifier to accomplish a current to voltage conversion. The circuit is a transimpedance function. The diode current is proportional to the light intensity striking it.

Bridge Sensor Linearization



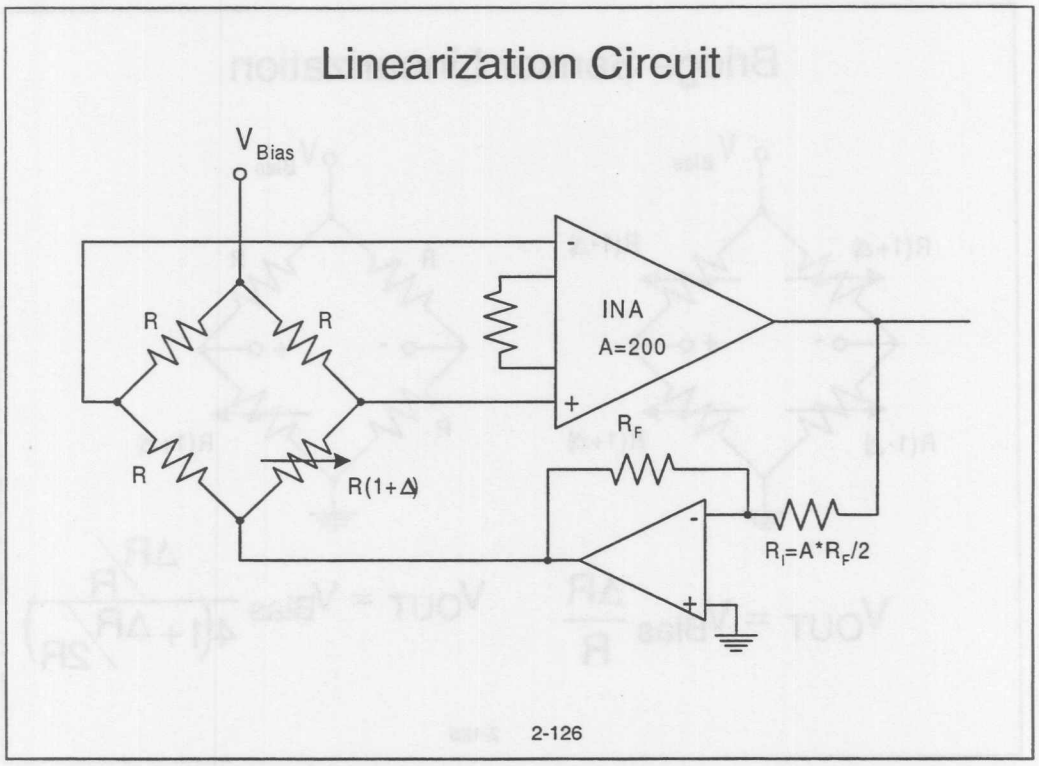
$$V_{OUT} = V_{Bias} \frac{\Delta R}{R}$$



$$V_{OUT} = V_{Bias} \frac{\Delta R/R}{4\left(1 + \Delta R/2R\right)}$$

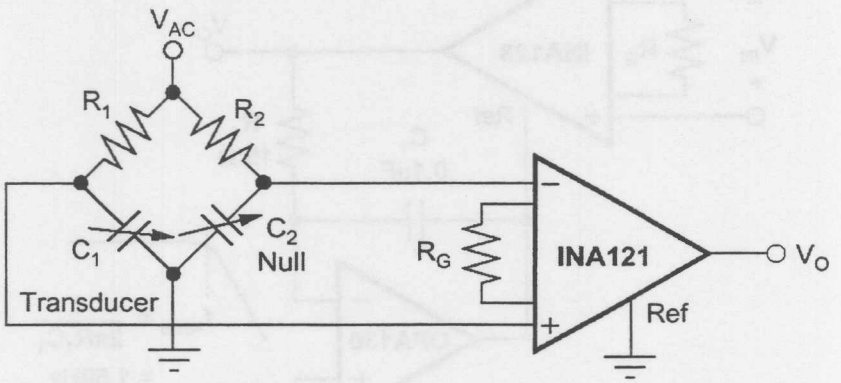
2-125

For a bridge sensor with four active elements shown on the left the transfer function is linear. When only one element is active as shown on the right the transfer function is not linear.



The signal from a sensor with only one active element can be made linear with the circuit shown. This circuit samples the output and adjusts the drive to the bridge. Single element bridges are not widely used however, this circuit is meaningful in that it illustrates the power of feedback to correct for sensor non-linearity.

Capacitive Bridge Transducer

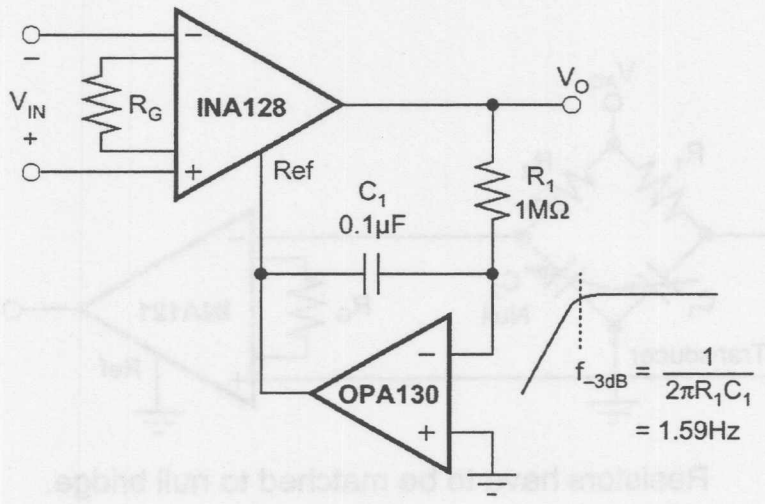


Resistors have to be matched to null bridge.

2-127

This application shows the balancing of a capacitance bridge. The null capacitor C_2 is adjusted to balance the bridge at the zero point. A path is provided for the bias current through the resistors in the top of the bridge.

Quasi AC-Coupled INA

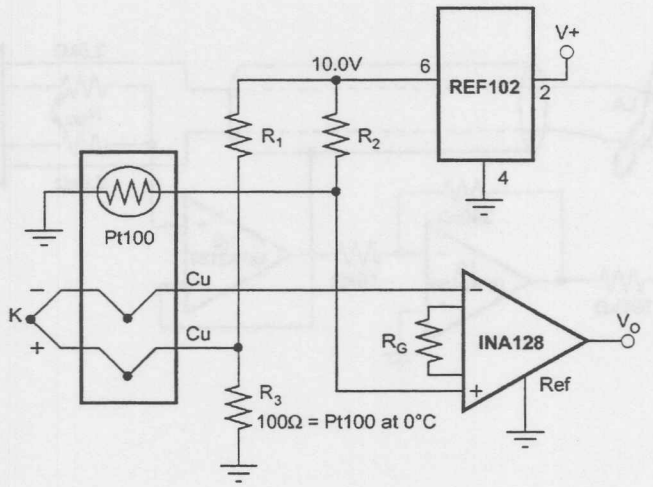


2-128

For those situations where the differential signal has a significant DC component this circuit will remove it. The advantage is that an equivalent series capacitor would be much larger, costly and could distort the signal. By using an op amp to integrate the average output voltage and drive it to zero the DC component is removed.

TC Amp with CJC

Thermocouple Amplifier With RTD Cold Junction Compensation

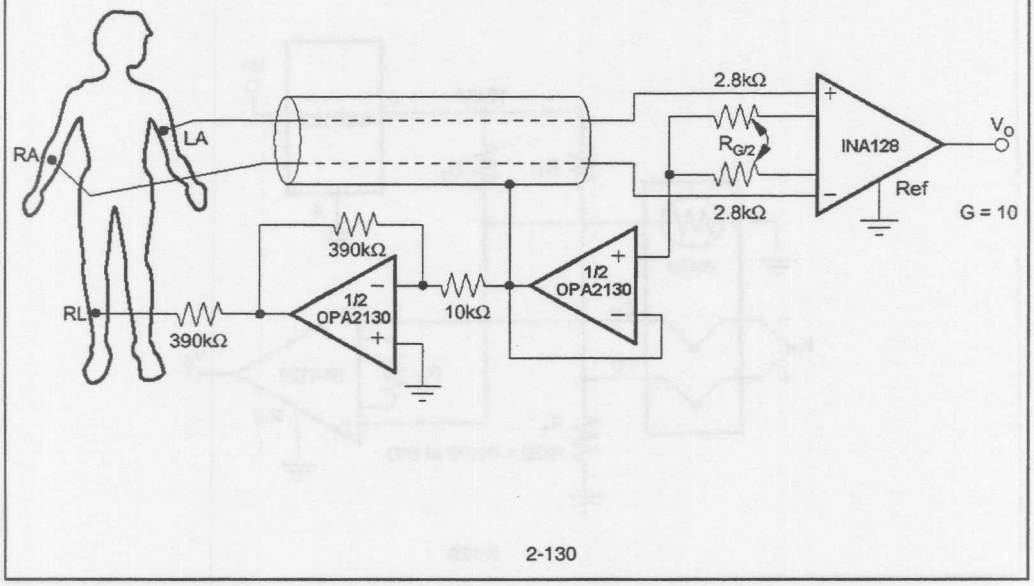


2-129

An INA can be the ideal amplifier to process a thermocouple signal. To determine the temperature at the TC point it is necessary to subtract the voltage that corresponds to the temperature at the junction block. The subtraction of two signals is accomplished with an INA. The 100 ohm RTD is used to determine the cold junction temperature.

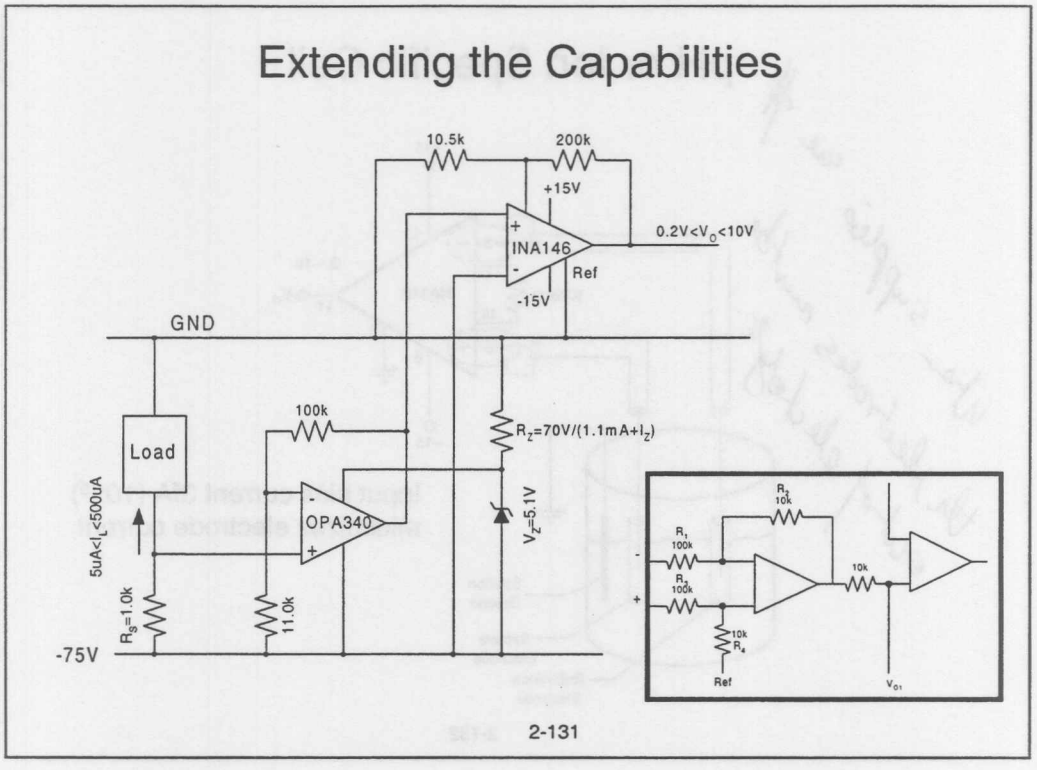
ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (μV/°C)	R_1, R_2
E	+ Chromel – Constantan	58.5	66.5kΩ
J	+ Iron – Constantan	50.2	76.8kΩ
K	+ Chromel – Alumel	39.4	97.6kΩ
T	+ Copper – Constantan	38.0	102kΩ

ECG With Right-Leg Drive



2-130

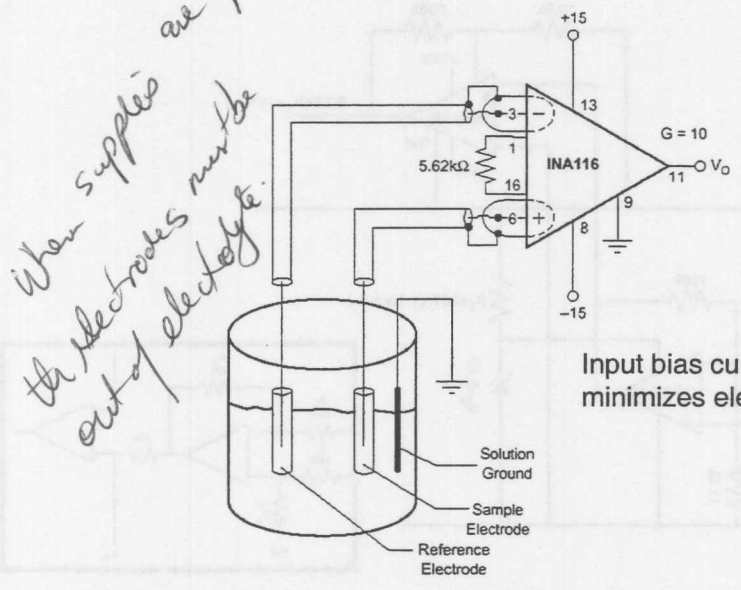
This application demonstrates a technique for canceling large common mode signal so that small cardiac signals can be processed. The common mode voltage exists at the midpoint of the gain set resistance on the INA. Buffering that potential allows the shield to be driven such as to minimize the voltage between it an either wire in the cable. The buffered signal is inverted and gained up to be applied to the patient to cancel the common mode noise.



In this application there is a 1.0k sense resistor in a supply line at -75V. With 5 to 500μA through the sense resistor the signal to be measured is 5 to 500μV. Direct application of a high CMV diff amp would be less than ideal because the sense resistor would upset the CMR of the diff amp. High input impedance INAs will not work because none have the CMV range necessary.

It is possible to use a RRIO op amp to buffer the signal and amplify it to so that it can be applied to the high CMV diff amp. A zener regulated supply will work for the op amp.

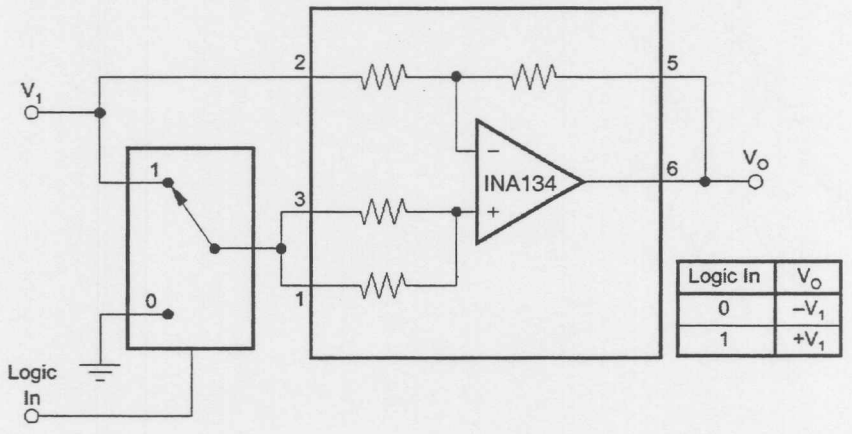
pH or Ion Specific Cell



2-132

Direct measurement of the pH of a solution is possible with special electrodes. One requirement of this procedure is that virtually no current flow in the electrodes. The INA116 has a bias current of 3fA ($3*10^{-15}$A). If significant current is allowed to flow the electrodes become polarized and the accuracy is lost. The bias current path is through the solution to the solution ground electrode.

Digitally Controlled Gain = ±1



2-133

This circuit changes from a non-inverting gain of one to an inverting gain of one under control of a logic signal. With the switch in the 0 position the gain is -1. With the switch in the 1 position the amplifier is in a gain of +2-1 for a net gain of +1. This can work as a synchronous demodulator.

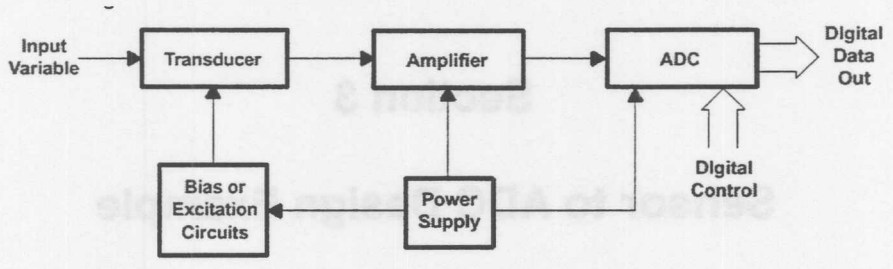
Section 3

Sensor to ADC Design Example

3-1

This section describes the design of a sensor to ADC system. The sensor measures temperature, and the measurement is interfaced into an ADC selected by the systems engineering department.

Block Diagram of Transducer Measurement System



3-2

The temperature sensor (transducer) must be excited with a bias to perform per the specification. As is often the case, the bias comes from a reference circuit which supplies reference voltages for the system. The ADC is selected prior to this design, and because we can not modify the selection, we just work with it. The amplifier is designed last because it is the interface between the sensor and ADC.

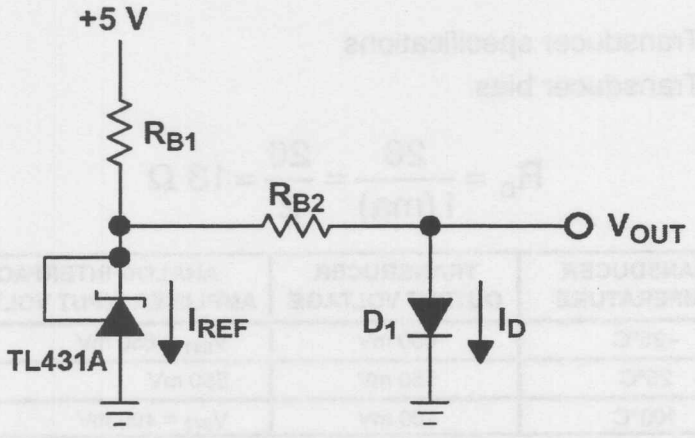
SNR = 6.02n + 1.76

n = 12

= 72dB

OP AMP SNR ⇒ 72dB.

Transducer Considerations
Reference and Bias Circuit



3-3

A shunt diode was chosen as the reference because it can do the job at the least cost. More accurate references exist, and we would like to sell them to you because they cost more, but they are not justified but the accuracy requirements of this design. R_{B1} is selected to supply the reference and temperature sensing diode current. R_{B2} is selected to limit the diode current to the specification value, and worst case calculations show that the diode current is always within specification. The ~~reference~~ output voltage also acts as a bias voltage for the op amp, but this current is negligible so it isn't considered here.

Transducer Output Voltage

- Transducer specifications
- Transducer bias

$$R_D = \frac{26}{I\,(ma)} = \frac{26}{2} = 13\ \Omega$$

TRANSDUCER TEMPERATURE	TRANSDUCER OUTPUT VOLTAGE	ANALOG INTERFACE AMPLIFIER INPUT VOLTAGE
–25°C	650 mV	V_{IN1} = 650 mV
25°C	550 mV	550 mV
100°C	400 mV	V_{IN2} = 400 mV

3-4

When the temperature transducer is biased correctly it yields the temperature/voltage relationship shown in the table. There is an error term that is not accounted for in the table, but it does not enter into the design at this point because the error is adjusted out in the final circuit. Correct bias insures that the transducer meets its specifications, so the design meets specification. The transducer output resistance can form a voltage divider with the amplifier's input resistance, thus it is calculated here as a parameter to be used in the op amp selection.

ADC Considerations

Resolution vs. Accuracy

RESOLUTION does not imply **ACCURACY**

nor does

ACCURACY imply **RESOLUTION**

3-5

The selection of the ADC involves several factors. These factors are often system rather than circuit design concerns because the ADC may be used for several applications within a design by multiplexing. The design type determines if missing codes are allowable and what degree of monotonicity is required. System specifications identify the required accuracy, and the circuit must conform to the system specifications.

The interface decision, serial or parallel, is dependent on the processor or logic rather than circuit restraints. Parallel interfaces are faster but they require lots of interface lines, while serial interfaces are slower with fewer interface lines. Internal references are generally preferred to reduce component count, but external references have higher precision.

ADC Converter Topologies

Topology	Sample Rate	Resolution
SAR	1Msps	8-16 bits
Sigma-Delta	50Ksps	12-24 bits
Pipeline	80Msps	8-14 bits
Flash	500Msps	8-12 bits

3-6

Resolution and accuracy are not identical. An ADC may have 16 bits resolution, i.e. the output can be resolved into 2^{16} bits, but the ADC or circuit accuracy may be much less than the resolution because internal or external error sources. An example is illustrated by the equivalent number of bits formula. The ADC may be advertised as 12 bits, but at the actual operating frequency it may be accurate to 10 bits.

The Input During Conversion

Consider an ADC without a S/H amplifier

Maximum frequency sine wave can be accurately digitized?

Input signal $e_{in}(t) = \frac{E_{FS}}{2}\sin(2\pi ft)$

Slew Rate $\frac{de_{in}}{dt} = 2\pi f \frac{E_{FS}}{2}\cos(2\pi ft)$

Max SR at cos=1 $f = \frac{\frac{de_{in}}{dt}}{\pi E_{FS}}$

In terms of ADC $f = \frac{\frac{1}{2}LSB}{\pi T(2^N LSB)}$

12 bit, 1μsec ADC $f = \frac{1}{\pi 2^{12+1}(1\mu sec)} = 38.9Hz$

3-7

There are many different methods of constructing an ADC. The SAR converter initially assumes a midscale value and does a loop calculation to determine the value of each bit. This type converter is accurate but slow because it requires n-bit loop calculations to produce an n-bit ADC. The sigma delta ADC has an integrating feedback loop that drives errors to zero if enough calculations are made. Typically the sigma delta ADC is the slowest ADC because it over samples by such a large margin, but it is the most accurate ADC.

A flash converter consists of a string of comparators with an input of each comparator connected to a resistive voltage divider fed by a precision voltage reference. The input voltage is connected to the other comparator inputs, so the output of the comparators is low until the input voltage equals the reference voltage where the output voltage goes high. This type of flash ADC has no protection features, and it requires 2^{n-1} comparators. A pipeline converter contains a small flash converter, and it applies the flash converter to the input signal in steps. Each step yields part of the output solution, so the answer comes out in pipeline form. A flash is the fastest ADC and the pipeline is the next fastest ADC.

ADC Characteristics

- System Engineer Selected: TLV2544
- Rin = 20 kΩ
- VOS = ± 150 mV
- Drift = 800 ppm
- Sampling Frequency = 100 kHz

ADC INPUT VOLTAGE	DIGITAL OUTPUT	ANALOG AMPLIFIER OUTPUT VOLTAGE
0 V	000000000000	V_{OUT1} = 0 V
4 V	111111111111	V_{OUT2} = 4 V

3-8

The system engineer selected the TLV2544 ADC because it can be multiplexed over meets the system requirements, and it can be used in the single shot mode where the ADC input resistance is 20K. The effective sampling rate after allowing for the multiplexing is 100kHz. The data rate is less than 1Hz, thus because of the high sampling rate a single pole low pass filter serves the anti-aliasing function.

The offset voltage is expressed in mV because it can be adjusted out, but the ADC drift is expressed as bits because it is an error that decreases accuracy. The ADC output voltage range sets the required amplifier input voltage range because the input signal must cover the complete ADC input range to obtain maximum accuracy.

Op Amp Selection

DESIGN SPECIFICATION	ESTIMATED VALUE	CANDIDATE OP AMP: TLV247X
R_{IN}	10^6 (13) Ω	10^{12} Ω
V_T	350 mV to 700 mV	–0.2 V to 5.2 V
R_{OUT}	20k.	1.8 Ω
V_{INADC}	0 V to 4 V	0.15 V to 4.85 V
V_{OS}	—	2.2 mV
I_B	—	100 pA
V_N	—	$\frac{28\ nV}{\sqrt{Hz}}$
I_N	—	$\frac{0.39\ pA}{\sqrt{Hz}}$
Analog noise	—	10 mV
k_{SVR}	—	63 dB

3-9

The TLV247x is a candidate op amp for the amplifier job, thus its salient specifications are listed in the table. A million times the sensing diode resistance yields an acceptable error from voltage divider action between the diode and op amp input. The op amp has $10^{12}\Omega$ input resistance so divider action is minimal. The transducer output voltage, VT, is 350mV to 700mV, and this range is overlapped by the op amp's input voltage range, hence no error results from this source. The op amp's output resistance is 1.8Ω. This resistance forms a voltage divider with the ADC input resistance (20kΩ), and the voltage divider action is minimal because of the resistances values.

The ADC expects to see an input voltage of 0V to 4V, and the op amp output voltage is guaranteed to span the output voltage range of 0.15V to 4.85V. This problem could be solved by increasing the op amp power supply voltage, by choosing another op amp, or by shifting the ADC input up. None of these solutions are required because the high ADC input resistance enables us to use the nominal value of V_{OL} = 85mV, and the resultant error is acceptable. Offset voltages and currents would not be considered because they can be adjusted out, but they are so small that they add very little error to the design.

The noise specifications for the op amp are excellent but meaningless in this design because the cable noise overshadows them. Power supply noise rejection is acceptable, thus this op amp is selected for the design.

Amplifier Input / Output Voltages

INPUT VOLTAGE	OUTPUT VOLTAGES	
V_{IN1} = 650 mV	V_{OUT1} = 0 V	1st pair of data points
V_{IN2} = 400 mV	V_{OUT2} = 4 V	2nd pair of data points

$$Y = mX + b$$

$$4 = 0.4m + b$$

$$0 = 0.65m + b$$

$$4 = 0.4\left(\frac{-b}{0.65}\right) + b$$

$$V_{OUT} = -16V_{IN} + 10.4$$

3-10

The op amp input voltage (sensor output voltage) and op amp output voltage (ADC input voltage range) are matched up as two data points on a straight line. Then the equation of a straight line and simultaneous equations are employed to obtain the final equation for the op amp. The case three circuit is selected for the design, and component values are calculated as previously shown.

Offset and Gain Error Budget

ERROR PARAMETER	INTERCEPT	GAIN	DRIFT
V_{REF}	±25 mV		
V_{REF} drift			7.41 mV ≈ 8 LSB
Transducer offset		± 50 mV	
Transducer R_{OUT}			13 Ω ≈ 0 LSB
ADC reference		± 150 mV	1 LSB
Total unadjusted ADC error			2 LSB
Gain error		1.6 LSB	
ADC drift			4 LSB
V_{OS} op amp	2.2 mV		
I_B op amp	100 pA		
V_N op amp			$\frac{28\ nV}{\sqrt{Hz}}$ ≈ 1 LSB
I_N op amp			$\frac{139\ pA}{\sqrt{Hz}}$ ≈ 0 LSB
V_{NPS} PS noise			10 mV ≈ 2 LSB
R_{OUT} op amp			1.8 Ω ≈ 0 LSB
$V_{OUT\ LOW}$ op amp			70 mV ≈ 72 LSB
Total error			~~18 LSB~~ 96 LSB

3-11

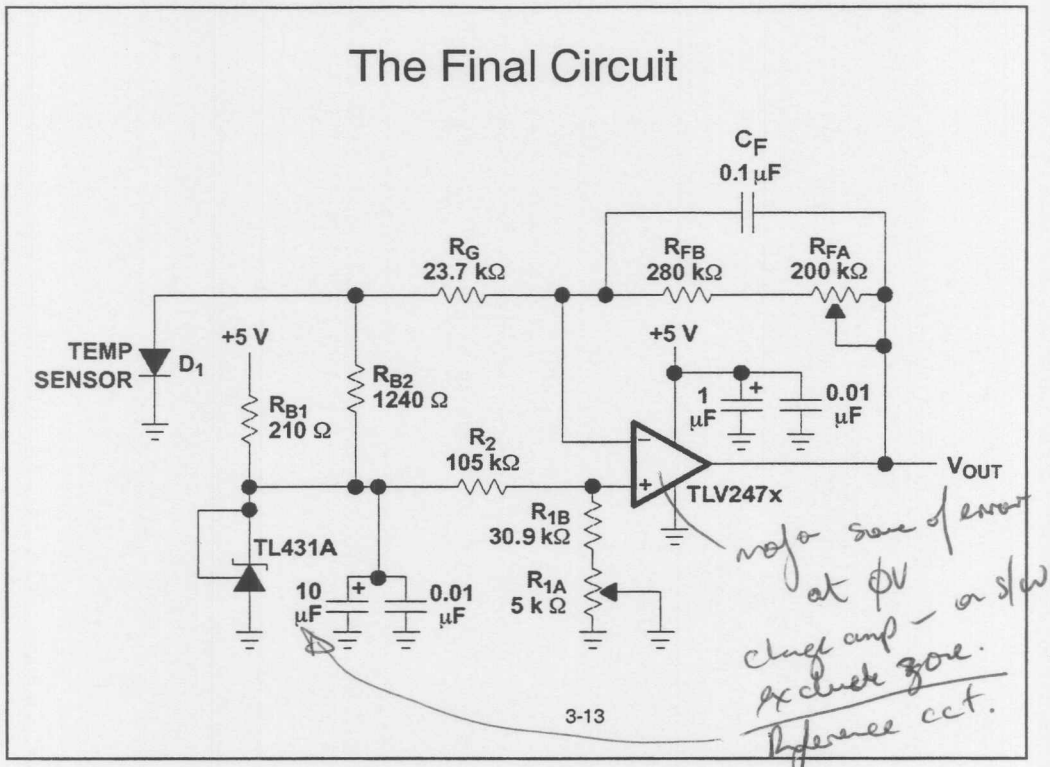
The offset errors are tabulated in the intercept column. The gain errors are tabulated in the gain column. After the ideal component values are calculated potentiometer values are chosen so the offset and gain errors can be adjusted out. Notice that drift errors accumulate and subtract from the accuracy of the design.

Anti-Aliasing Circuit

- Sampling Frequency = 100 kHz
- Data Frequency < 1Hz
- Cable Noise = 10 mV
- Very relaxed requirements
- Add parallel feedback capacitor CF = 0.1 μF

3-12

Because of the relative difference between the sampling and data frequencies, and because the cable noise over shadows other noise concerns, picking an anti-aliasing filter is easy. Use a feedback capacitor across the feedback resistor because this acts as a low pass filter and improves stability. Select the value of the feedback capacitance as 0.1μF because this value is available in ceramic, stable, and inexpensive.



Two reference supply filter capacitors and two decoupling capacitors are shown in the final schematic because practical consideration require them. Splitting the value of RG and adding a capacitor at the junction of the two resistors can filter the sensor diode output. This decision is normally reserved until the actual hardware testing is completed. Notice that two adjustment resistors have been added to the design.

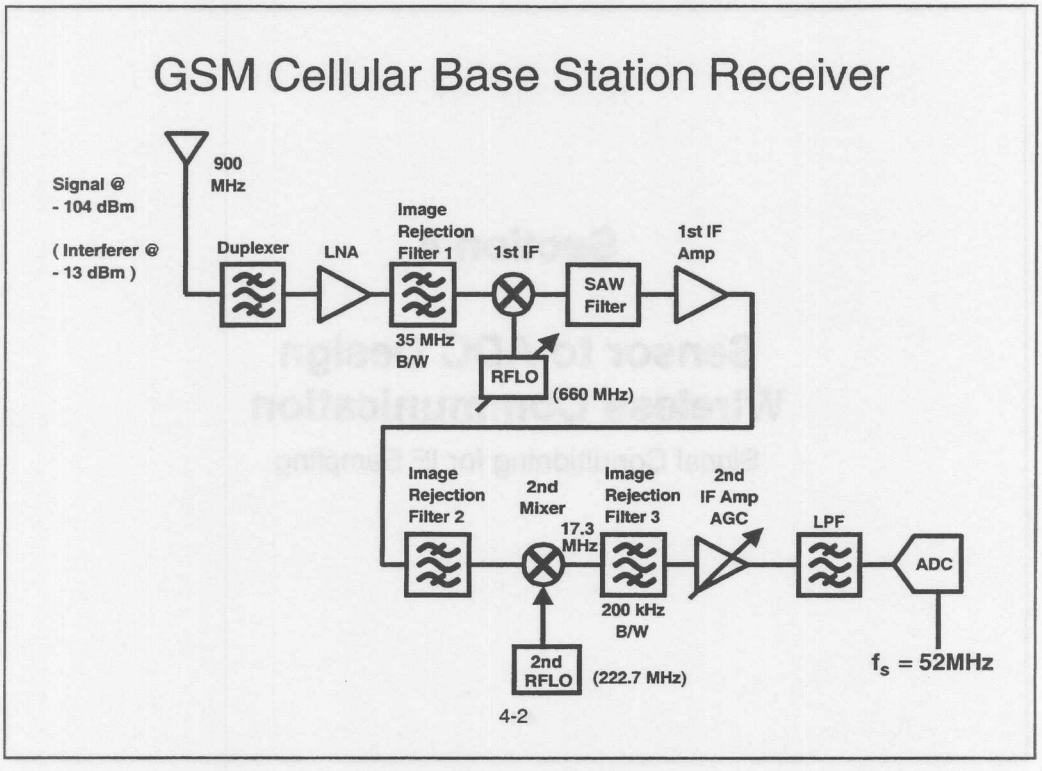
Section 4

Sensor to ADC Design
Wireless Communication

Signal Conditioning for IF Sampling

4-1

High-speed op amps are used extensively in wireless communications. These amplifiers usually operate below 500MHz, and often they operate at 25MHz and below. Applications for high-speed op amps include filtering circuits, IF amplifiers, cable drivers, ADC drivers, and mixers.



Several stages with different IF frequencies are used in a dual IF receiver. The receiver converts the RF input to a base band signal. Receiver performance is measured in terms of receiver sensitivity, which is the ratio of the power of the desired baseband signal to the power of all undesirable signals (measured at the ADC output).

The 900MHz RF signal is received by the antenna and amplified by the low noise amplifier (LNA). The signal is then bandpass filtered to obtain image rejection and selectivity. The first mixer converts the band limited RF and local oscillator frequency (660MHz) into a difference frequency (240MHz). The first stage IF filter selects the difference frequency while rejecting noise, sum, original, and spurious frequencies. The first stage IF frequency passes through another image rejection filter and is mixed with the second local oscillator (222.7MHz). The next image rejection filter constrains the IF choice to a range of 10 to 20MHz. The signal is then amplified, gain controlled, and passed through a low pass filter to the ADC.

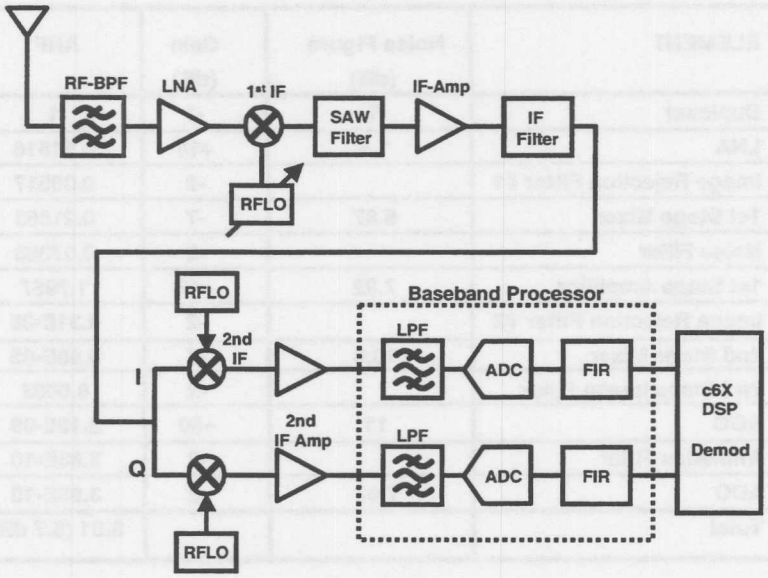
GSM Receiver Block-System Budget

ELEMENT	Noise Figure (dB)	Gain (dB)	ANF*
Duplexer	1	-1	1
LNA	1.6	+18	0.51616
Image Rejection Filter #1		-2	0.00517
1st Stage Mixer	9.87	-7	0.21853
Noise Filter		-2	0.07363
1st Stage Amplifier	7.92	+49	1.7957
Image Rejection Filter #2		-2	4.31E-06
2nd Stage Mixer	10.8	-7	5.68E-05
2nd Stage Image Filter		-2	0.0009
AGC	11	+50	2.16E-09
Anti-alias Filter		-2	3.83E-10
ADC	7.63	-2	3.83E-10
Total			3.61 (5.7 dB)

4-3

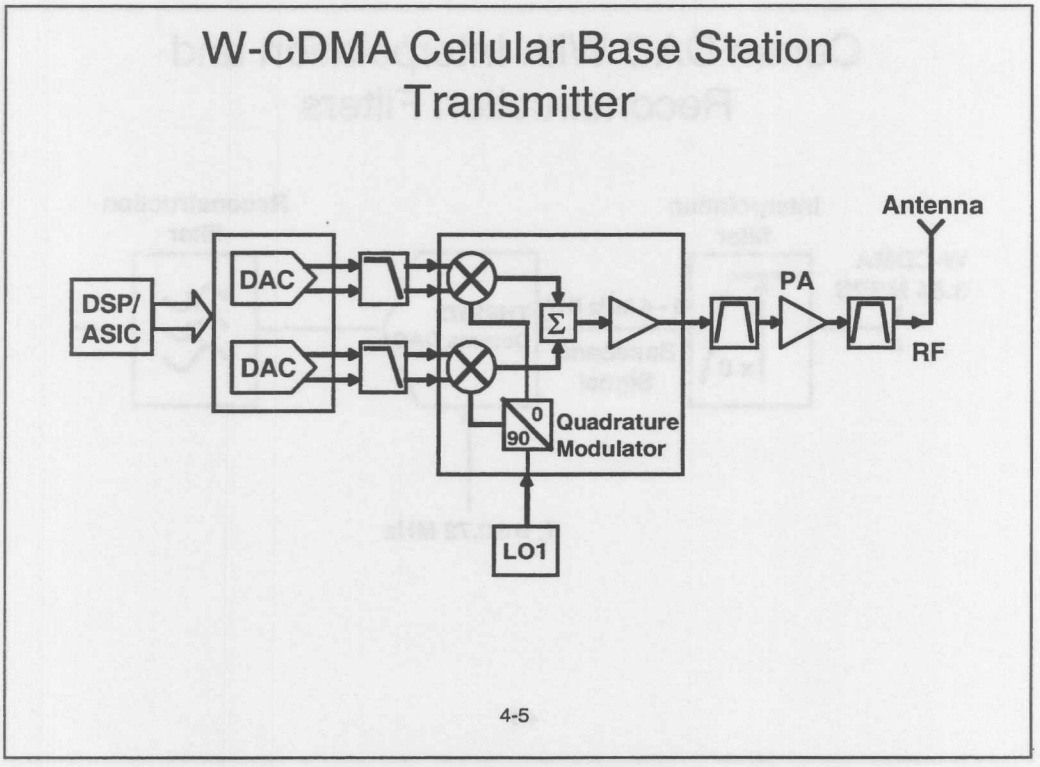
This table is a tabulation of the contribution of each stage to the system level error budget for a typical GSM receiver.

Software Configurable Dual IF Receiver



4-4

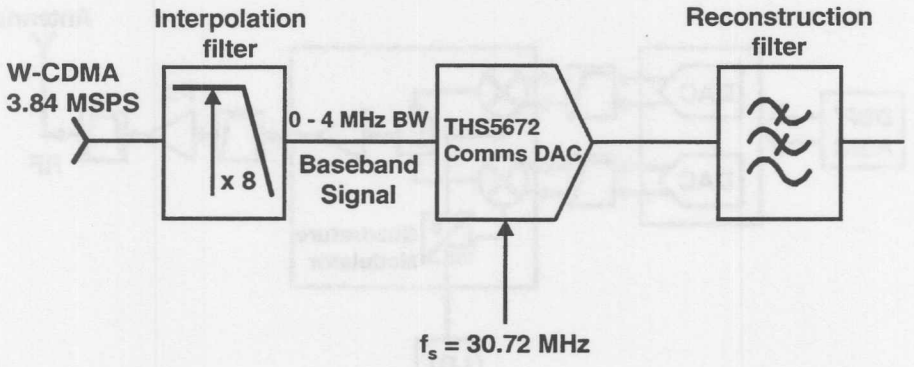
The digital signal processor (DSP) enables more flexibility in the receiver. The DSP allows a single receiver to access several different wireless systems through changes in software configuration.



A voiceband coder-decoder (CODEC), op amps and DSP are used to digitize and band limit the audio signal. The digitized signal is compressed to the desired data rate in hardware or by software implemented on a DSP. Redundancy (error correction) , encryption, and modulation (QPSK for W-CDMA or GMSK for GSM) are added to the compressed digitized signal.

The DAC converts the modulated bit stream to analog; often two DACs are used, one for the I channel and one the Q channel. The modulator block converts the baseband I and Q signal to the appropriate carrier frequency, typically 864MHz. The up converted signal is amplified by the power amp (PA) which drives the RF amplifier and antenna. The RF amplifier is a large signal amplifier with power gain on the order of 50% for GSM and 30% for code division multiple access (CDMA).

Comm DAC With Interpolation and Reconstruction Filters



4-6

Assuming that the modulated bit stream is a 3.84 MSPS W-CMDA signal, for 8x interpolation, the sampling clock frequency must be 30.72MHz. The reconstruction filter at the DAC output is usually a high order Bessel or elliptic filter, and it filters the DAC transitions out the analog signal.

ADC/DAC Considerations

- DC non-linearity is not important
- Effective number of bits ENOB
- Spurious Free dynamic range SFDR
- Total Harmonic Distortion THD
- Signal-to-noise ratio SNR
- Sampling Rate
- Full scale range FSR

4-7

The dc non-linearity performance is not nearly as important in a communications ADC as it is in an instrumentation ADC because signal are band limited. The dynamic performance of the ADC is critical in communications applications. The overall receiver system specifications depend heavily on ADC dynamic performance parameters such as the effective number of bits (ENOB). ENOB is usually measured and specified at the system operating frequency, so it is a real performance measurement.

Spurious free dynamic range (SFDR) determines the ADC's ability to separate an incoming signal from ADC noise spikes. Total harmonic distortion (THD) is a measure of the distortion that the ADC adds to the signal. Signal-to noise ratio (SNR) includes ADC noise and noise from other sources.

ADC Requirements for Processing GSM Signal

- $SNR_{THERMAL}$= 9dB for GSM-900
- Process gain required =24dB (fS/BW)
- Selected ADC_{SNR}= 37dB better than thermal
- Baseband converter = 46dB
- SNR_{ADC} = (46-24) = 22dB
- ENOB (effective number of bits) = (SNR-1.76)/6.02 = 3.36 bits signal (4 bits required)
- Interferer = 40dB ≈ 6.3 bits

4-8

The mean squared quantization power is $P_{qn} = q_s^2/12R$ where q_s is the quantization step size and R is the ADC input resistance, typically 600Ω to 1000Ω. Communication ADCs similar to the THS1052 and THS1265 typically have a full-scale range (FSR) of 1Vp-p to 2Vp-p. Based on the assumption of a 50Ω input/output termination, the quantization noise power for a 12 bit, 65MSPS ADC is –74dBm. The receiver noise power in a noise-limited receiver can be computed as the thermal noise power in the given receiver BW plus the receiver noise figure.

For 200kHz BW (GSM channel), T_A = 25°C, and 4 to 6dB NF the receiver noise power is –115dBm. To boost the receiver noise to the quantization noise power level requires a gain of 42dB. The smallest 1% bit error-rate (BER) for GSM-900 is –104dBm, thus the SNR at baseband due to the thermal noise component is given by $SNR_{THERMAL} = E_b/N_0$ = -104dBm +115dBm = 9dBm. For a raw BER to be 1% in a GSM system, testing and standard curves indicate that a baseband SNR of 9dB is needed for this performance.

The process gain is $G_p = f_S/BW = 52x10^6/200x10^3 = 2.6x10^2 = 24dB$ where the GSM channel BW is 200kHz and f_S is 52MHz (ADC sampling frequency). The converter noise at baseband should be much better than the radio noise (thermal noise plus process gain), hence the converter noise at baseband = SNR_{ADC} + process gain (G_p).

SNR_{ADC} is selected as 37dB better than $SNR_{THERMAL}$; baseband converter noise is 9dB + 37dB = 45dB. SNR_{ADC} required to meet the GSM-900 standard is (46-24)dB = 22dB. The ENOB of the ADC must be = (SNR-1.76)/6.02 ≅ 4 bits. Assuming that the filter attenuates the interferer by 50dB, the interferer drops from 113dBm to –53dBm, or 40dB above the GSM signal. The number of bits required to accommodate the interferer is 40dB/6db/bit =6.3 bits. Six bits are required to accommodate the interferer, 4 bits are required for the GSM signal, and 2 bits are required for headroom, so we need a 12 bit converter.

Op Amp Requirements

Parameter	Value	Units	OPA685
Noise Voltage	2.7 to 8	nV/√Hz	2.7 Nv/√Hz
Noise Current	1 to 30	pA /√Hz	11.9 pA/√Hz
THD	70 to 95	dBc	82 dBc
Slew Rate	260 to 3500	V/μV	1700 V/μs
Small Signal Bandwidth	200 to 600	MHz	900 MHz
Large Signal Bandwidth	≥100	MHz	135 MHz
Common-mode input voltage	3	V	+/- 2.9V
Supply Voltage	+/- 5	V	+/- 5V
Settling Time	8 to 20	ns	15 ns
Output Current	40 to 100	mA	80 mA
Output Impedance	≤20	ohm	0.02 Ω
PSRR	-60	dB	-64 dB
CMRR	-70	dB	50
Input Offset Voltage	10	mV (typ)	+/-5 mV

4-10

The SFDR and IMD are the key ADC/DAC parameters that influence op amp selection. A minimum requirement is that the op amp's SFDR or IMD, measured at the operating frequency, be 5dB to 10dB better than the converter's equivalent specifications. A perfect 12 bit ADC has a SFDR or IMD of 72dB, and the op amp should have a SFDR or IMD of 77dB to 82dB. Fast settling time is mandatory because the ADC must settle within a fraction of an LSB in the ADC sampling time.

Low voltage systems are popular now, and the designer must be aware that ac specifications are only valid at the test supply voltage. Operating the op amp at different supply voltages changes their ac specifications.

Anti-Aliasing Filters for GSM

- Sampling clock (FS) aliases with HF noise to produce baseband noise
- Filter cutoff frequency (FC) equals maximum baseband frequency
- Must reduce out of band noise to < 1dB
- GSM--- ADCdB/ (FC-FM) = 72dB/(18-35)MHz = 72dB/OCTAVE =12 poles

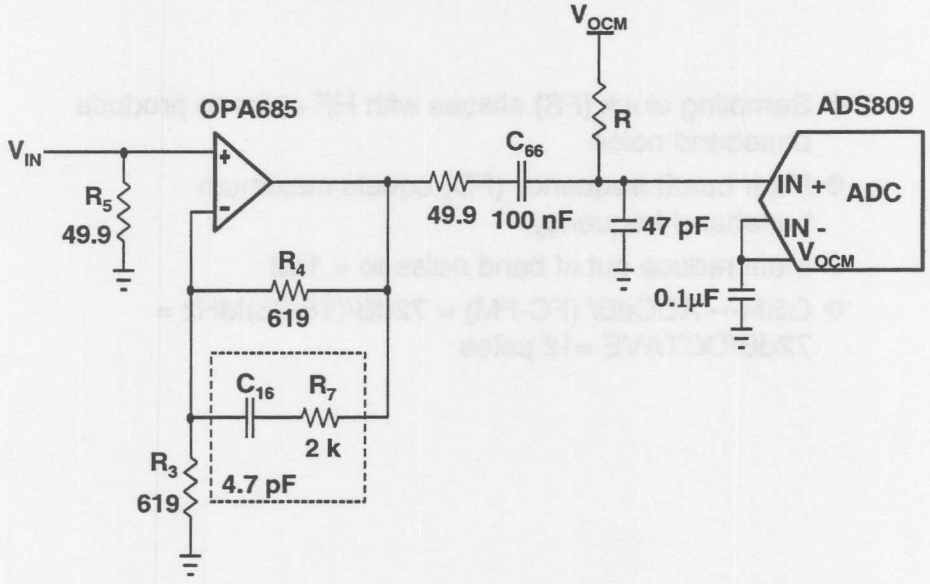
4-11

Spurious signals (>f_S/2) must be prevented from getting into the ADC (sampling at Nyquist rate f_s) where they cause aliasing errors in the ADC output. A suitable anti-alias low pass filter placed before the ADC prevents frequency components capable of aliasing from reaching the ADC. The anti-alias filter cutoff frequency (f_C)is set to the highest baseband frequency of interest (f_{MAX}) so that $f_C = f_{MAX}$. The Nyquist sampling theorem requires the ADC sampling rate t be twice the maximum baseband frequency ($f_S = 2f_{MAX}$). Only an ideal "brickwall" filter can meet these criteria of filtering out all aliasing frequencies, thus reality dictates $f_C > 2f_{MAX}$.

The highest signal frequency of interest sets the cutoff frequency. Suppose the input frequency to be sampled is 12 bit accuracy with a sampling frequency of 52MHz, and the IF frequency is 17MHz, then an 18MHz filter –3dB cutoff frequency could be chosen. All frequencies above the Nyquist frequency should be attenuated to < 1/2LSB. Only the frequencies above the ADC's resolution limit are a problem; i. e., f_{ALIAS} = (52-17) = 35 MHz. The frequency roll off is 18 to 35 MHz (about an octave) and the required attenuation is 72dB (12 bit ADC), so approximately a 12^{th} order filter is required. Practical anti-aliasing filters are limited to 6^{th} order, and that is why f_S usually exceeds f_{MAX} by a large margin.

See Errata

ADC Single Ended Driver Circuit



4-12

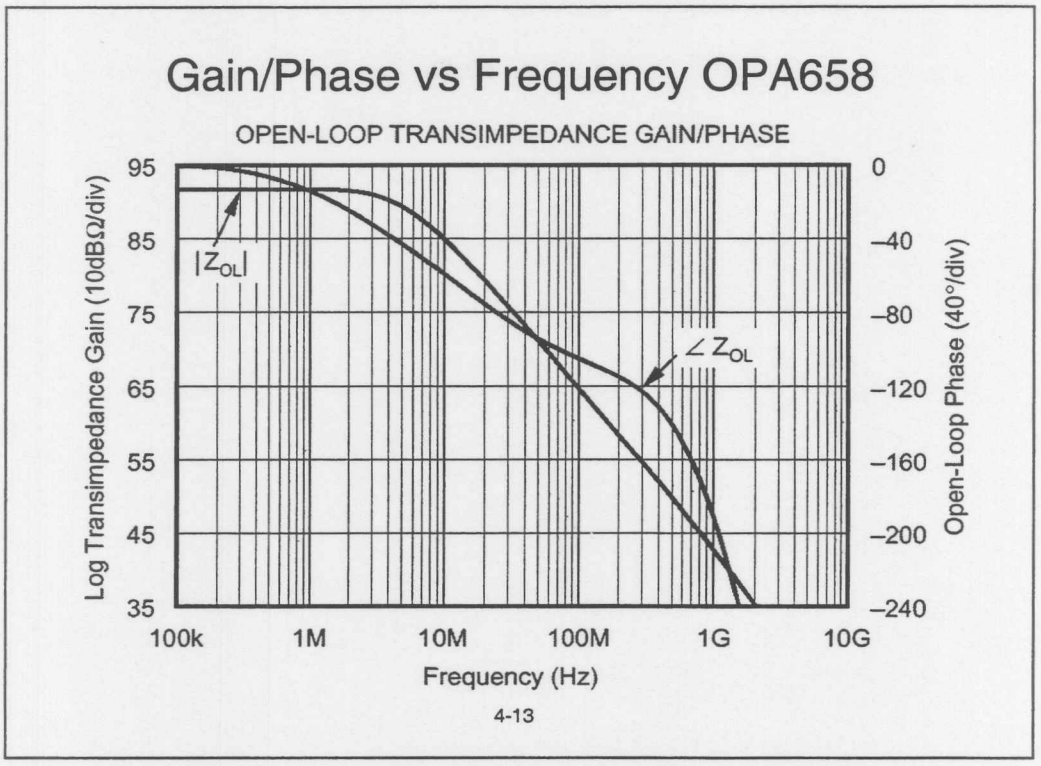
An op amp voltage follower circuit is often used to interface the external precision voltage reference supplying the ADC/DAC. V_{IN} is the output from a precision voltage reference such as Thaler Corp. VRE3050. The low pass filter formed by R_1 and C_1 eliminates noise coming from the reference and buffer. The –3dB corner frequency (f_C) of the filter is $1/2\pi C_1R_1$, and the transfer function for the circuit is given below.

$$\frac{V_O}{V_{IN}} = \frac{1 + sC_1R_1}{\left(s^2 + \frac{sC_2R_2}{C_1R_1C_2R_2} + \frac{1}{C_1R_1C_2R_2}\right)C_1R_1C_2R_2}$$

When $C_2R_2 = 2C_1R_1$ the resultant poles are:

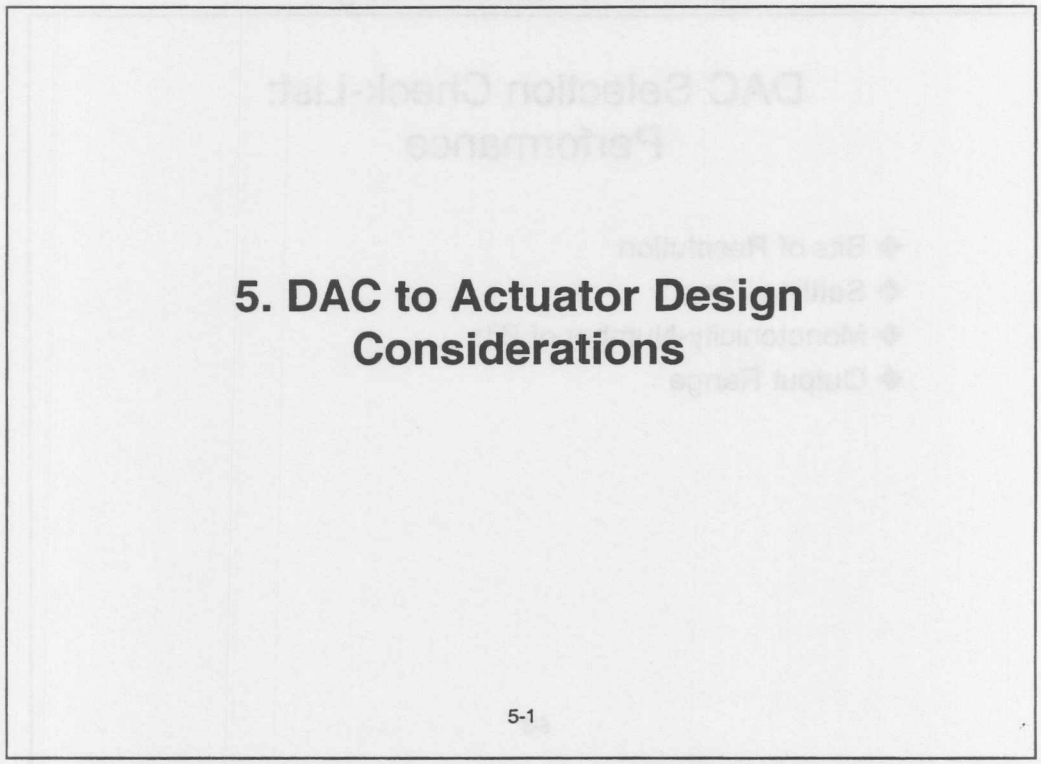
$$P_1, P_2 = -\frac{1}{2C_1R_1} \pm j\frac{1}{2C_1R_1}$$

See Errata



Design example; Let C_1 = 1.2μF and R_1 = 42.2Ω, and C_2's value should be approximately 5% of C_1"s value, so C_2 = .047μF and R_2 = 2.15kΩ. The calculated –3dB BW is 3.1kHz, and this value agrees with the frequency response plot. This circuit is an excellent selection for driving large capacitive loads because C_1 adds to the load capacitance, and the zero containing C_2 stabilizes the circuit.

see Op Amps Book.



DAC to Actuator Design Considerations. Taking a signal from the sensor through a processor and converting it to produce results in the real world.

DAC Selection Check-List: Performance

- Bits of Resolution
- Settling Time
- Monotonicity-Number of Bits
- Output Range

5-2

There are four primary areas of performance that are of concern:

1. How much resolution is required for the application, how fine of a step is needed
2. The settling time, how quick do things have to be done
3. Monotonicity, or increasing change in applied digital word; the output must either stay the same or increase - this is very important for servo applications where we're closing the loop, adjusting the output of our DAC, measuring the results through another system and then deciding whether to increase or decrease our word to the DAC, to position a part in the right location
4. Output range, select from a 0-5V, ±5V, ±10V signal range. This section is going to take that limited output range signal and convert it into a useful high-voltage, high-current signal, precision current signal, to actually get the work done.

DAC Selection Check-List Features

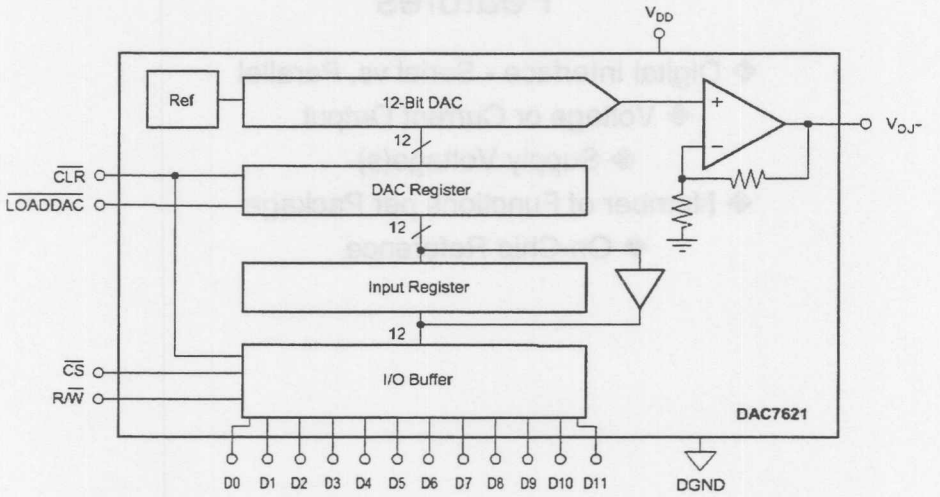
- ◆ Digital Interface - Serial vs. Parallel
- ◆ Voltage or Current Output
- ◆ Supply Voltage(s)
- ◆ Number of Functions per Package
- ◆ On-Chip Reference

5-3

This is a list of the DAC features that are considered in selecting a DAC.

- Serial ports are usually in short supply on embedded controllers.
- Almost all DAC are voltage out now. Older designs and very high speed DACs may still be current out devices but that is rare.
- Supply voltage is always a concern
- DACs are available in singles, duals, quads and octals.
- Some DACs have on chip reference.
- From the analog signal conditioning the major concern is the output voltage.

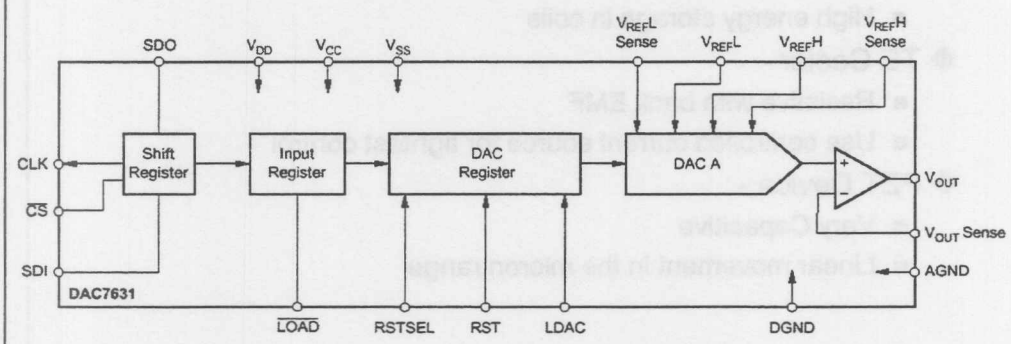
12 Bit, Voltage Output DAC



5-4

A 12 bit, parallel input DAC with voltage output. This has the feedback resistors included around the output op amp. With this circuit the feedback resistor are matched and will track with temperature. A voltage reference is on chip.

16 Bit, Voltage Output DAC



5-5

This is a 16 bit, serial input DAC. The output op amp inverting input node is brought to a pin so that it can be included in the application circuit and compensate for board losses if needed. A voltage reference is not included.

Actuator Characteristics

- Motor/Solenoid -
  - Inductive
  - High energy storage in coils
- TE Cooler -
  - Resistive with back EMF
  - Use controlled current source for tightest control
- PZT Device -
  - Very Capacitive
  - Linear movement in the micron range

5-6

Looking at the other end of the system; what is to be done with this signal? Are we going to move something, maybe a motor; drive a motor or move a solenoid, adjust a valve with a solenoid for partial closing of the valve? Solenoids and motors are inductive and can have a energy stored in the coils. This becomes significant when calculating the stress on the output transistor of the op amp that's driving the motor. A motor has constant torque with constant current. To control the torque drive it with a current source.

The TE cooler, thermoelectric cooler is finding wide application in DWDM, Dense Wave Division Multiplexing, keeping the lasers at a constant temperature. TE coolers rely on the Peltier effect, which perhaps is more familiar in terms of the Seabeck effect. That is the phenomenon seen in thermocouples. Two dissimilar metals at different temperatures will develop a current flow through the circuit. Conversely if a current is driven through a circuit of dissimilar metals it will cause heat flow or energy flow. It can use this as a heater/cooler to maintain a constant temperature.

These parts look like resistors with a back EMF; because I've got the junction to different temperatures, I'm going to be generating a slight voltage there. The tightest control or the most accurate control can be accomplished when these are driven with a current source, and we'll do some considerable current source analysis here in a moment.

And finally we'll mention a piezoelectric device. A piezoelectric device is really a very big capacitor, so the DC current is actually zero. If DC current flows through the piezoelectric device the device is probably destroyed. It can, however, require high current out of the op amp to operate at high frequency. In order to change the voltage across the capacitor quickly requires current. Recall the expression that $I=C\,dV/dt$. The faster a voltage across a capacitor is changed, the more current it will take. These devices are used to obtain linear movement in the micron range, such as positioning mirrors and moving small elements.

Power Op Amp Application Circuits

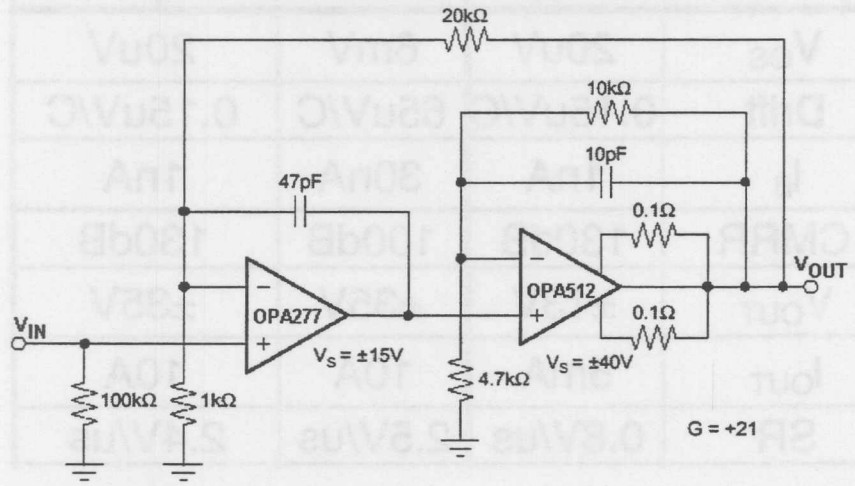
- Compound Amplifier
- Voltage to Current Converters
- Bridge Connected Amplifiers
- Parallel Amplifier Connections

5-8

Power op amp application circuits will make the bridge between the low-voltage, low-current output from a DAC and the required accurate high current, high voltage required by the output devices. Circuits include compound amplifiers, voltage-to-current converters, bridge-connected amplifiers and the parallel amplifier connection.

Compound Amplifier

Get improved precision of signal op amp



5-9

This circuit address the need for a power output stage with a precision input circuit. The combination is not available in one device. It is possible to combine the power capabilities of the OPA512 with the precision of the OPA277.

The OPA512 has the highest slew rate and therefore is operated within a local closed loop. The slower OPA277 is operated within the outer loop. The 47pF capacitor provides a small amount of phase shift to help stabilize the system.

Resulting Performance

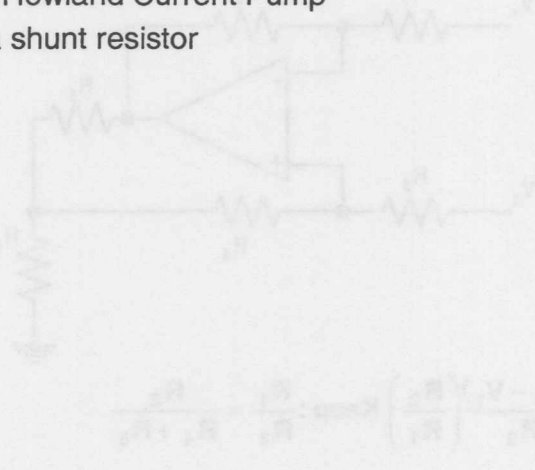
Parameter	OPA277	OPA512	Compound
V_{OS}	20uV	6mV	20uV
Drift	0.15uV/C	65uV/C	0.15uV/C
I_B	1nA	30nA	1nA
CMRR	130dB	100dB	130dB
V_{OUT}	±13V	±35V	±35V
I_{OUT}	5mA	10A	10A
SR	0.8V/us	2.5V/us	2.4V/us

5-10

The resulting performance of the compound amplifier shows that the front-end characteristics of the OPA277 are joined with the ±35V at 10A drive current capabilities out of the OPA512. The slew rate of the OPA277 is 0.8V/μs. That slew rate is gained up times three in the OPA512 so that there is an effective slew rate for the compound amplifier of 2.4V/μs.

Voltage to Current Converters

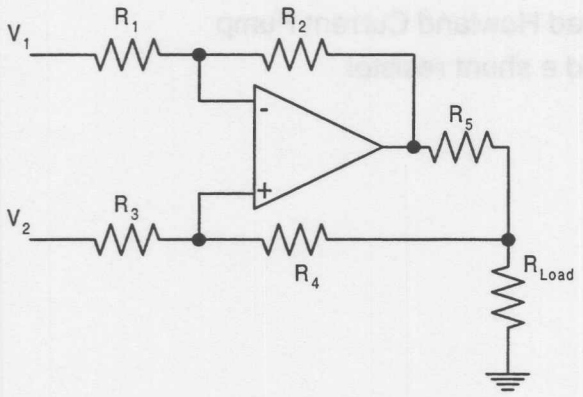
- Improved Howland Current Pump
- INA and a shunt resistor



5-11

In voltage-to-current converters there are two options: The improved Howland current pump, and using an INA with a shunt resistor.

The Improved Howland Current Pump



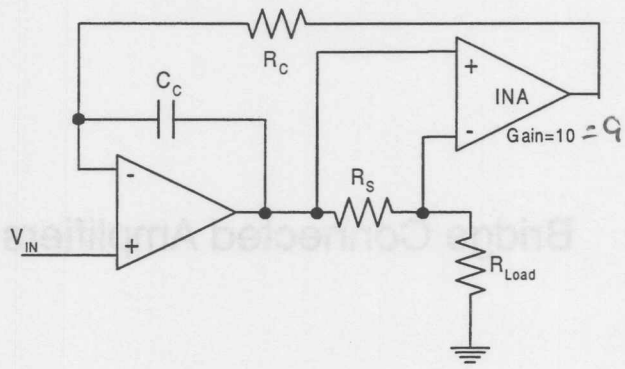
$$I_{Load} = \frac{(V_2 - V_1)}{R_5}\left(\frac{R_2}{R_1}\right) \quad \text{Keep}: \frac{R_1}{R_3} = \frac{R_2}{R_4 + R_5}$$

5-12

The improved Howland current pump uses the differential capabilities of the op amp to detect the voltage across R_5, the sense resistor, and use that to control the current flow through the load. The Howland current pump is a good compromise on getting controlled current into a grounded load. However, there are a couple of drawbacks here. Number one, the resistor ratios, R_1/ R_3 ratio, must equal the $R_2/(R_4+R_5)$ ratio to give us this transfer function. Even if build with 1% resistors accuracy will be on the order of 10 to 20 percent.

The accuracy issue is because of circuit interactions. The resultant circuit is still adequate for most motor drive applications.

Precision Current Control



$$I_{Load} = \frac{V_{IN}}{GR_S}$$

5-13

For a high precision current control take an instrumentation amplifier that has been talked about earlier today, connect it across the sense resistor as shown here, put in a gain to increase the effective value of the sense resistor and then feed that signal back to drive the op amp. It is required that the instrumentation amplifier have a higher bandwidth than the op amp.

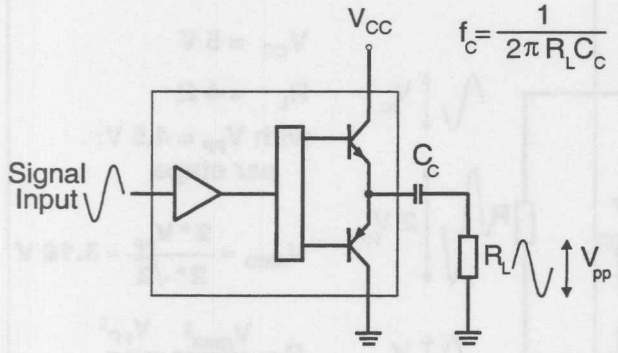
In some applications it may be necessary to put in a phase comp network as shown here with R_C and C_C to slow down the op amp.

Bridge Connected Amplifiers

5-14

Bridge connected op amps; very powerful - mind the pun - a very powerful operation here.

Output – Single Ended Configuration (SE)



V_{CC} = 5 V

R_L = 4 Ω

with V_{PP} = 4.5 V:

$$V_{RMS} = \frac{V_{PP}}{2 * \sqrt{2}} = 1.59V$$

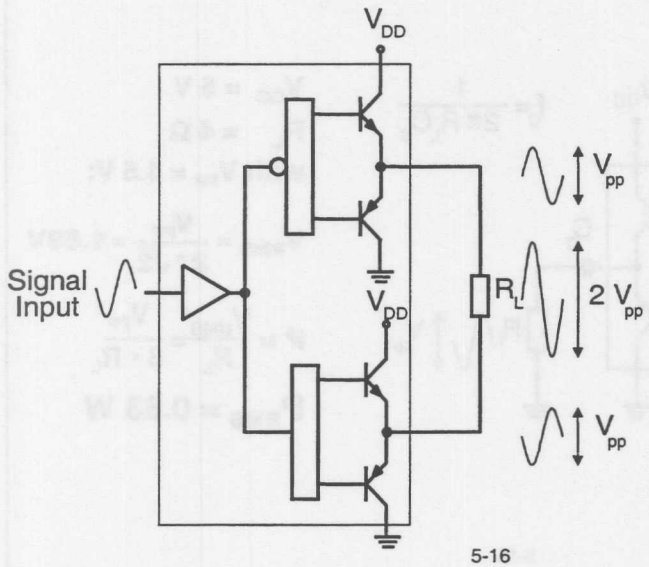
$$P = \frac{V_{RMS}^2}{R_L} = \frac{V_{PP}^2}{8 \cdot R_L}$$

P_{RMS} = 0.63 W

5-15

Consider the single-ended configuration. Given a 5V supply and a 4Ω load the amplifier can swing $4.5V_{PP}$ out. This results in a RMS power to the load of 5/8 of a watt.

Output – Bridge Tied Load Configuration (BTL)



V_{CC} = 5 V

R_L = 4 Ω

with V_{PP} = 4.5 V: per stage

$$V_{RMS} = \frac{2 * V_{pp}}{2 * \sqrt{2}} = 3.18\ V$$

$$P = \frac{V_{RMS}^2}{R_L} = \frac{V_{PP}^2}{2 \cdot R_L}$$

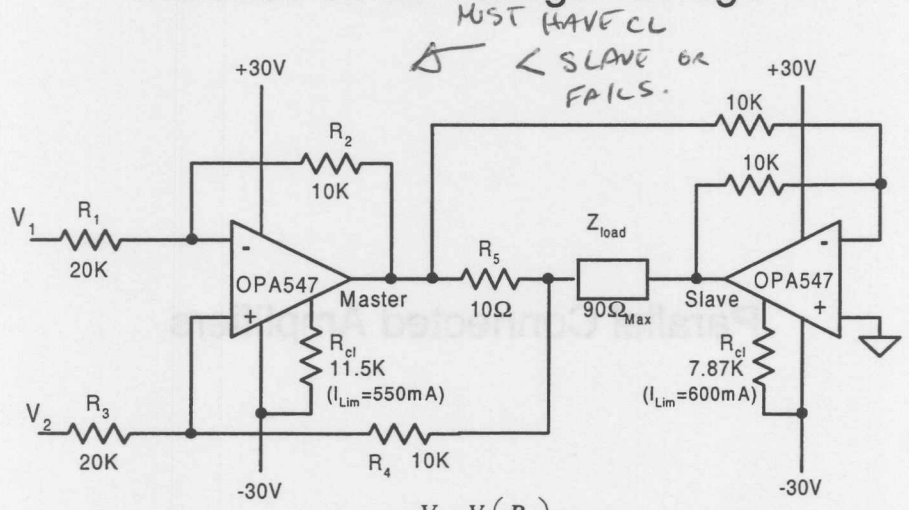
P_{RMS} = 2.53 W

5-16

If both ends of the load are available then put in a second stage to greatly increase the power to the load. The signal to the top stage is inverted from the bottom stage. The 5V, 4Ω, 4.5V_{PP} per stage parameters still apply. Because power goes with the square of the voltage, double the voltage and get four times the power. Now the RMS power, instead of being 5/8 of a watt, is going to be over 2.5W.

with Motor or solenoid.

Increase Drive Voltage - Bridge



$$I_L = \frac{V_2 - V_1}{R_5}\left(\frac{R_2}{R_1}\right); With R_1 = R_3 \;\&\; R_2 = R_4 + R_5$$

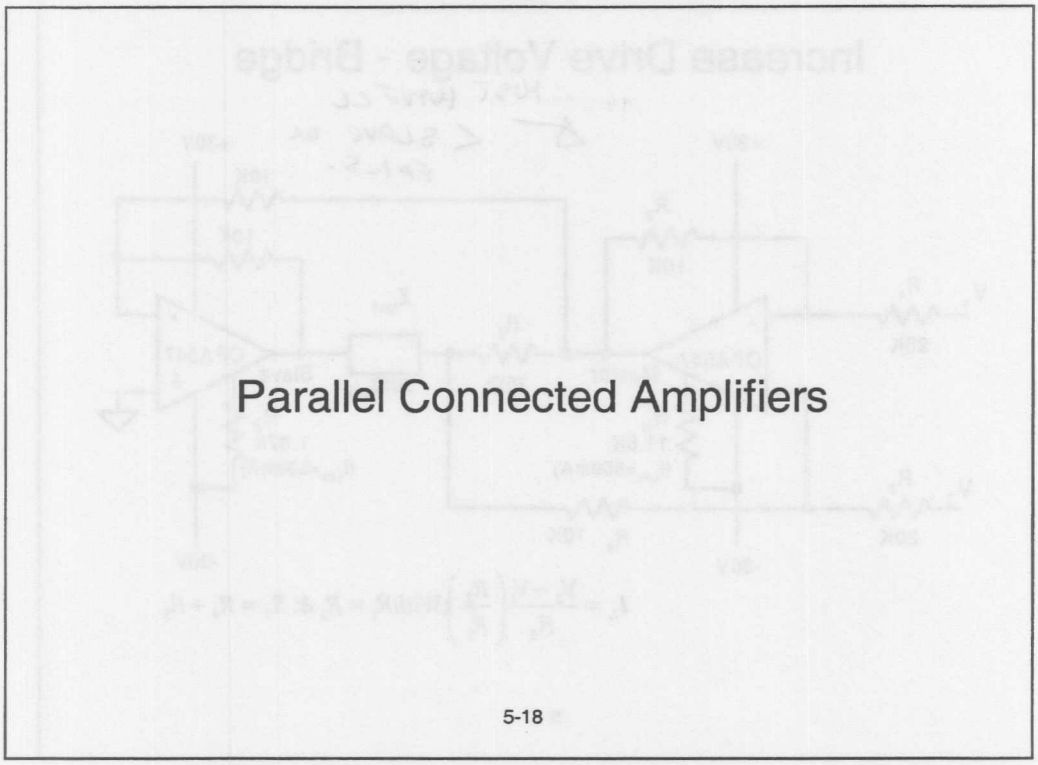
5-17

For more powerful bridge applications such as improved drive on a motor or a piezoelectric cell. This circuit is using the improved Howland current pump but any circuit on the master side can be done. It could be an active filter, a current source a plain gain stage. The master will establish an output voltage which will then be inverted with the slave amplifier. With voltage at the bridge of the center of the load does not move. Therefore, for power dissipation calculations and stability concerns operate the master side into half the normal load which is connected to ground. Any stability issues with the master side must be resolved before the slave side is added.

The OPA547 used here allows an external current limit set. This is an advantage because now the current limit on the slave can be set slightly higher than the limit current on the master.

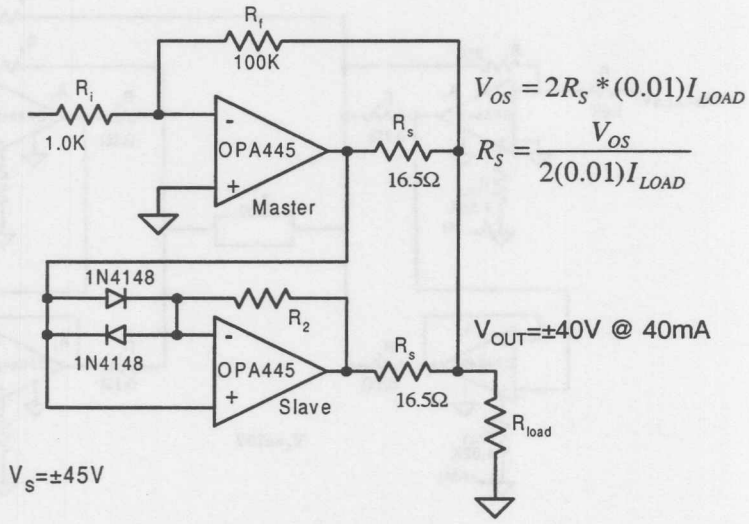
In a fault condition such as a stalled motor or shorted load which produces an over-current condition - the master will go into current limit first. As the master shuts down, the slave will follow, limiting the current output from both devices. If the slave is allowed to go into current limit first, the master would continue to drive and that will put considerable stress on the slave output stage. By staggering the current limit points as is done here, the amplifier drive circuit is protected.

A second advantage is that the slew rate of the circuit is twice that of the individual amplifier. As one side is going up at max slew rate the other side is going down at the same rate.



Increase current drive with parallel connected amplifiers.

Parallel to Increase Load Current

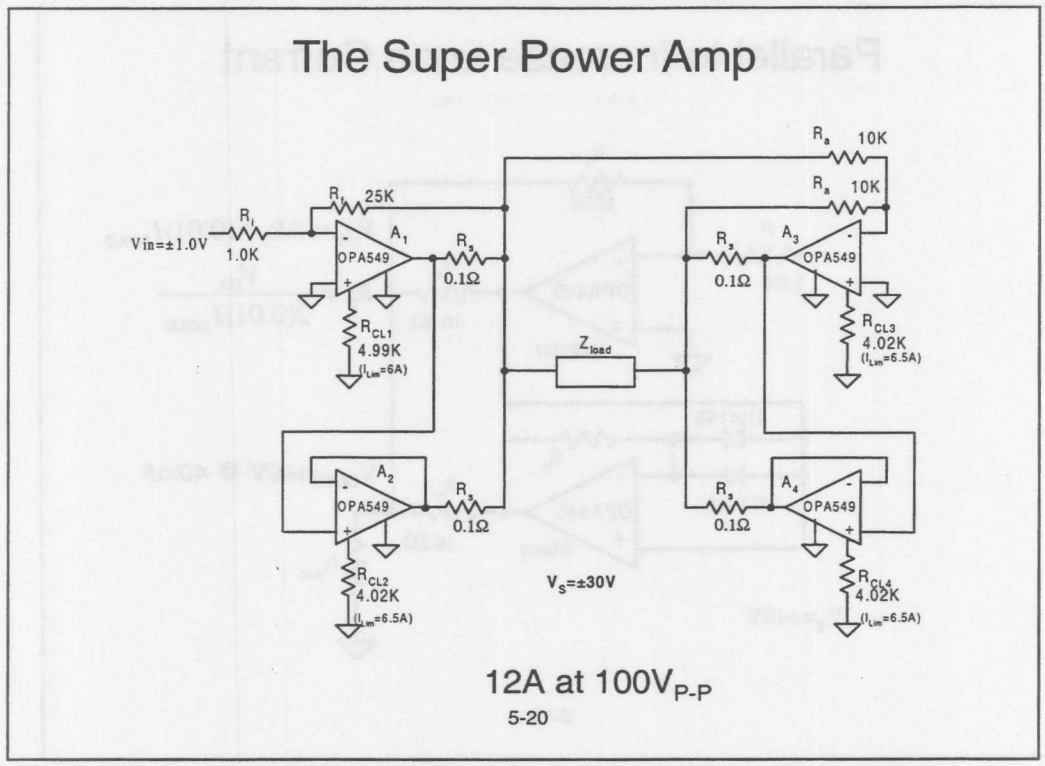


5-19

To increase load current, connect two amplifiers in parallel. There is no real limit to the number of amplifiers that can be connect in parallel. In this example the master op amp is operated in a gain of 100. The output of the master amplifier is applied to the slave, which is running in a non-inverted gain of 1.

With the two outputs connected together it is necessary to provide R_S to force the amplifiers to share the load. The output of the slave is going to be equal to the output of the master plus the voltage offset of the slave. That voltage is going to be impressed across both R_S resistors. Any current that flows in that loop is not flowing through the load. The nominal goal is limit that current to 1 percent of the load current. This gives the relationship shown on the slide.

The resistor, R_2, and the diodes are there because the OPA445 suffers from phase inversion; that is if the input is over driven to the negative rail, the output will flip to the positive rail. In this fault condition the amplifiers fighting against each other. The diodes and resistor prevent the overdrive.



For the super amplifier use four OPA549s, an 8A output op amp. Place two of them in parallel - A_1, A_2 on the left-hand side. A_1 is the master, running in a gain of 25. It is sharing the load with A_2 with each putting out 6A. That output voltage is connected to A_3, which is running as a bridge slave. The A_3 output is applied to A_4 which is run as a parallel slave. Total capability is 12A at $100V_{PP}$

The master is current-limited at 6A, all of the slaves at 6.5A.

Circuits like this with six amplifiers on each side of the bridge are not out of the question. That could result in a 50A-output device to be used to drive a stepper motor on a wafer-scanning station. This system will require a significant heat sink as there will be a significant quantity of heat generated in these op amps.

Power Op Amp Considerations

- Safe Operating Area (SOA)
- Heat Sinks
- Current Limit

5-21

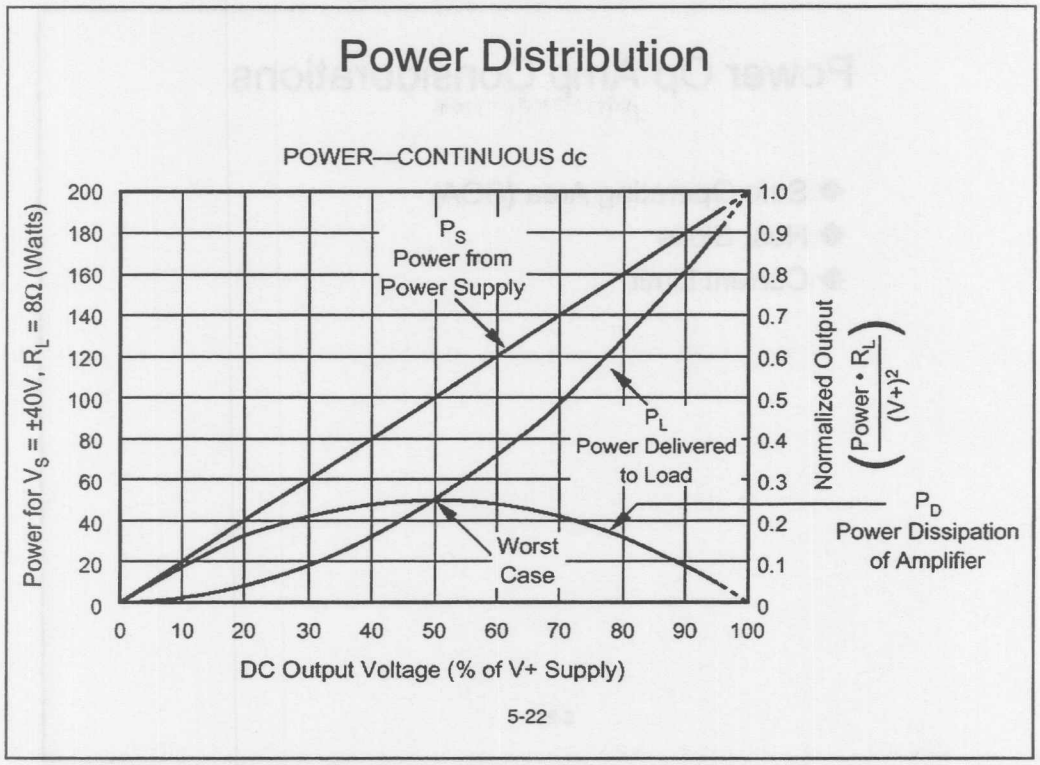
Power op amp considerations: Safe operating area, heat sinks, and limiting the current.

Application bulletins of interest:

MOUNTING CONSIDERATIONS FOR TO-3 PACKAGES - SBOA020

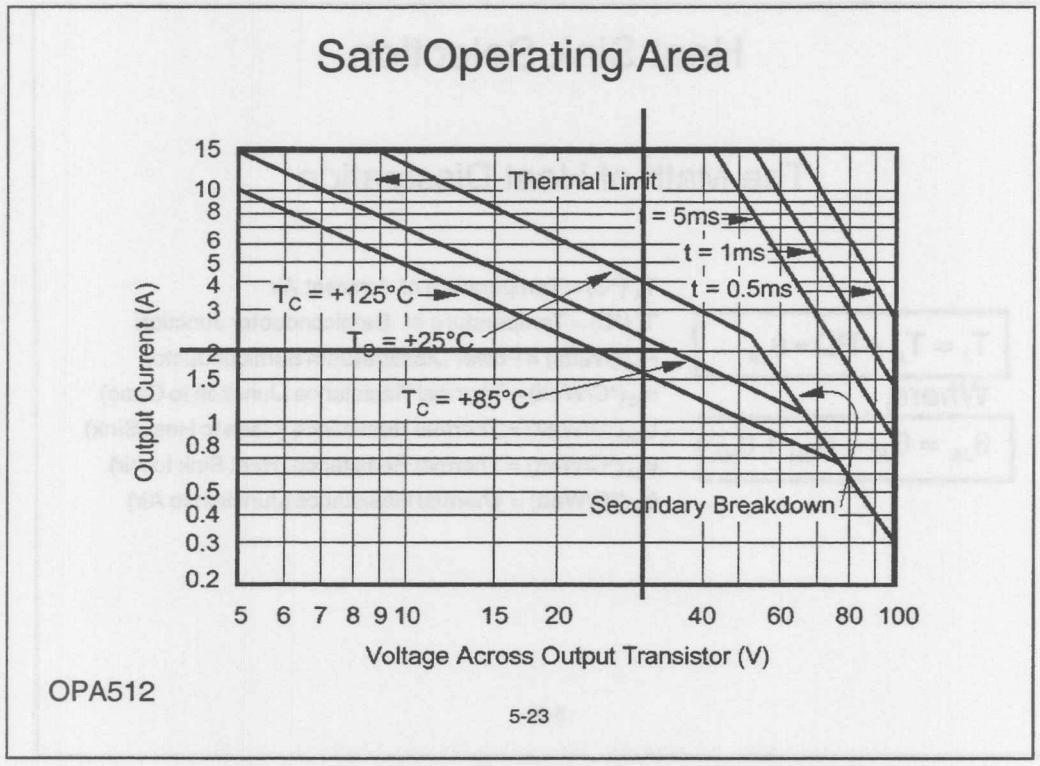
HEAT SINKING — TO-3 THERMAL MODEL - SBOA021

POWER AMPLIFIER STRESS AND POWER HANDLING LIMITATIONS - SBOA022



This is a plot of the power dissipation in the load and in the op amp as the load voltage goes from zero to maximum. Notice that the peak power in the amplifier is when the output voltage is at 50% of the supply rail. For heat sink requirements and Safe Operating Area (SOA) concerns this is the power to considered.

This is for a pure resistive load. As the load becomes more reactive this curve is going to shift. The power dissipated in the amplifier will go up at the higher outputs, and the peak will actually move closer to 60 or 70% of supply.



There is an upper limit to the stress that can be supported by the output devices of the amplifier. In this case the curves are for case temperatures of 25°C, 85°C and 125°C for the OPA512. These are lines of constant power. The EI product along any line is going to be a constant.

Notice the slope on the right-hand side marked secondary breakdown. This is zone of operation that is unique to bi-polar transistors where the device goes into thermal run away.

As an example, consider a situation with 30V developed across the output transistor at 2A into the load. To remain within the SOA it is necessary to maintain a case temperature of approximately 100°C. This means there will be a need for a pretty good-sized heat sink.

This op amp is a 15A device if the temperature at the case is 25°C or less and the voltage across the output transistor at 9V or less. Keeping 25°C at 9V times 15A or 135W dissipation in the amplifier. Notice the only concerned is with the power being dissipated in the amplifier; there is no concern with the power being dissipated in the load.

Heat Sink Selection

The Math of Heat Dissipation

$$T_J = T_A + PD \bullet \theta_{JA}$$

Where,

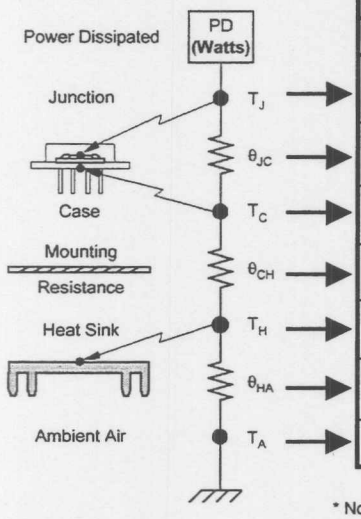
$$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$$

T_A (°C) = Temperature of Ambient Air
T_J (°C) = Temperature of Semiconductor Junction
PD (Watts) = Power Dissapated in Semiconductor
θ_{JC} (°C/Watt) = Thermal Resistance (Junction to Case)
θ_{CH} (°C/Watt) = Thermal Resistance (Case to Heat Sink)
θ_{HA} (°C/Watt) = Thermal Resistance (Heat Sink to Air)
θ_{JA} (°C/Watt) = Thermal Resistance (Junction to Air)

5-24

The design of a heat sink is based on some empirical measurements made by the heat sink manufacturer, and some empirical measurements made within the enclosure of the final system. The actual mathematics is straightforward. it looks like a simple circuit. Take temperature to be the equivalent of voltage, thermal resistance is now just a simple resistor and the power is considered the same as current. Now this looks like a linear circuit, and in fact the resistances add linearly.

The Equivalent Circuit



Units	High Power Application		Low Power Application	
Watts	100W	10W	10W	1W
°C	145	37*	158*	39
°C /Watt	0.8	0.8	0.8	0.8
°C	65	29	150	38
°C /Watt	0.1	0.1	0.5	0.5
°C	55	28	145	37
°C/Watt	0.3	0.3	12	12
°C	25	25	25	25

* Note the difference in junction temperature that thermal resistance can make even when operating at the same power level.

5-25

This chart compares the performance of two different heat sinks, each at two different power levels. To analyze the equivalent circuit start at ground or at the ambient temperature. Multiply the power by the heat sink thermal resistance, add that to the ambient temperature to find the temperature at the interface between the heat sink and the case.

Now, the power has to pass through the mounting resistance and that resistance is either 0.1 or 0.5°C/W.

With the 10W dissipation can either result in 37°C junction temperature or 158°C junction temperature. This really points out the advantage of getting a highly-efficient heat sink to get the heat out of the device and into the air.

It can be noted that certain things like putting a fan on the heat sink will significantly increase its effectiveness; just open your PC and look at the cooler on the Pentium chip.

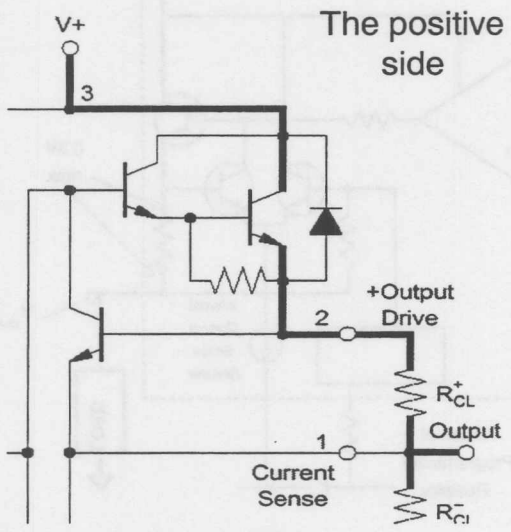
Limiting the Load Current

- Sense I_{load}
- If greater than set point.....
- Reduce base/gate drive

5-26

Limiting load current, really simple: sense the current in the load. If it's greater than a set point, reduce the base or gate drive to the output devices.

Current Limit Circuit-Old Style

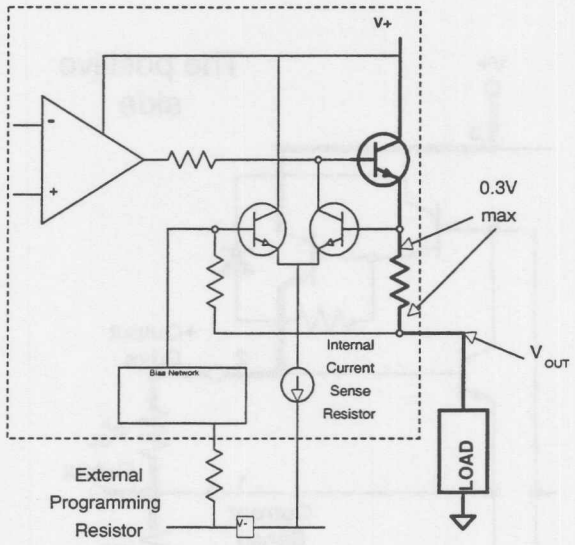


This is the classical current limit circuit. The power flows from the positive supply down through the output device through the current limit set resistor, which is outside of the package, to the load. As the current through the load and through the current limit resistor increases the voltage from Pin 2 to Pin 1 increases. When the voltage reaches 0.7V, nominally the V_{BE} drop of the transistor, it turns on the transistor. And it starts robbing base drive from the output devices. This forms a simple linear control loop.

There are short comings in this circuit. The V_{BE} of the limiting transistor is not a very closely-controlled parameter. From one device to the next within a product a 10- or 20-percent variation could be expected. Another issue is that the V_{BE} drop of a transistor is temperature-dependent. It has a temperature coefficient of -2.2 mV/°C. As the part gets warmer, the current limit is reduced. At least it's going in the right direction.

It should be noted that the current limit resistors are large; they have to carry the full load current load. To change current limit set point requires changing resistors, and these are typically on the order of 0.1 to 0.01Ω. Also the resistance of the copper trace on the board may become significant, as well as socket contact resistance.

Current Limit Circuit-New



5-28

This shows a new current limit circuit available in the OPA547, OPA548, and OPA549. The sense resistor is built inside the package. It is sized to develop about a 0.3V max. That sense voltage is applied to a differential pair. On the other side of the differential pair is applied a bias or set point voltage. When the current through the load becomes high enough, the difference is detected in the differential pair. When it gets high enough, then the differential pair starts robbing the base drive from the output device. This has the advantage that the current limit set point is determined by an external resistor which is simply a signal resistor, it doesn't have to be a big power resistor.

The current limit point can be set by adjusting the voltage on that pin, doesn't have to be a resistor. It can be a voltage from a DAC or a current source.

It is now possible to design a digitally-controlled power supply. Given two DACs, one to set the voltage and the other to set the current limit. Total digital control on a power supply. And further, this part runs nicely in current limit so there's no real degradation in performance, and get an accuracy of 10-percent.

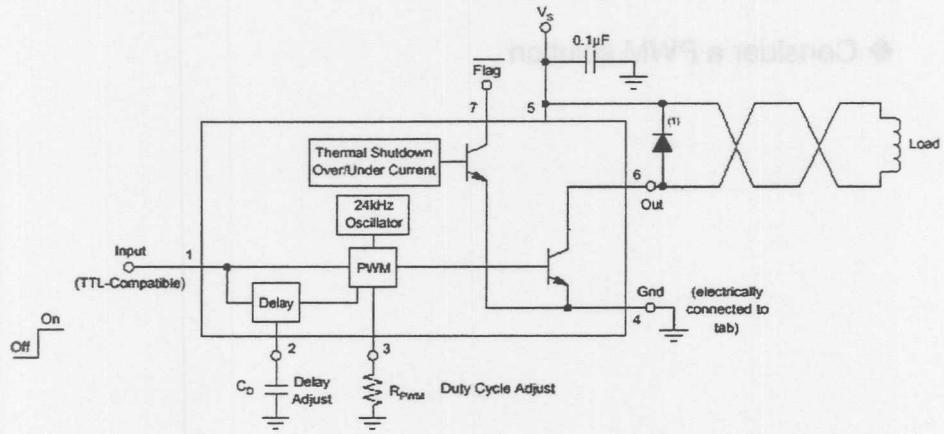
An Alternate Way to Drive

- Consider a PWM solution

5-29

When looking at alternate ways to drive, consider a PWM solution sometimes.

PWM Solenoid Drivers



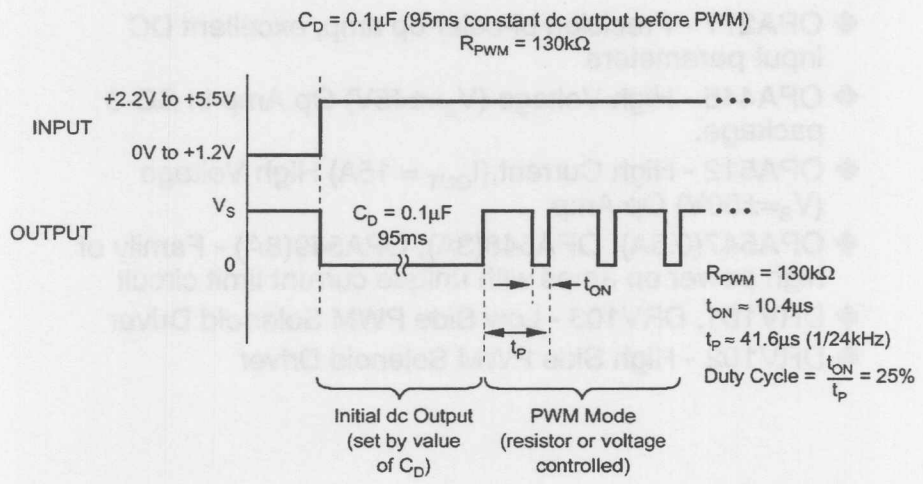
5-30

An ideal solenoid driver applies maximum current to pull the armature in and then drops the current to a lower hold-in value. This gets the best performance from the solenoid while causing the minimum heat in the coil.

The DRV101 shown here allows the user to set the full current time with the selected capacitor and then the duty cycle with the resistor. Turn-on and turn-off are controlled with the signal at pin 1.

The signal at pin 3 needn't be a resistor; it can be a voltage source or a current source. Therefore, it is possible to put this inside a control loop and drive pin 3 with a DAC signal. It is possible to accomplish proportional control over solenoid opening by the pulse-width duty cycle from this driver.

Timing Diagram



5-31

The output waveform of the DRV101. The delay time or time of full on is set by the value of CD. The PWM duty cycle is set by the value of the RDC.

With these devices the power dissipated in the device is minimal. When the device is off the voltage drop across it is full supply but the current through it is zero. When the part is on the current through it is high but the voltage across is is small. In both cases the EI product is near zero and therefore the power lost in the device is very small.

Devices Used in the Examples

- OPA277 - Precision bi-polar op amp, excellent DC input parameters
- OPA445 - High Voltage (V_S=±45V) Op Amp in SO-8 package.
- OPA512 - High Current,(I_{OUT} = 15A) High Voltage (V_S=±50V) Op Amp
- OPA547(0.5A), OPA548(3A), OPA549(8A) - Family of high power op amps with unique current limit circuit
- DRV101, DRV103 - Low Side PWM Solenoid Driver
- DRV102 - High Side PWM Solenoid Driver

5-32

Data sheets are available for these parts on the web at www.ti.com .

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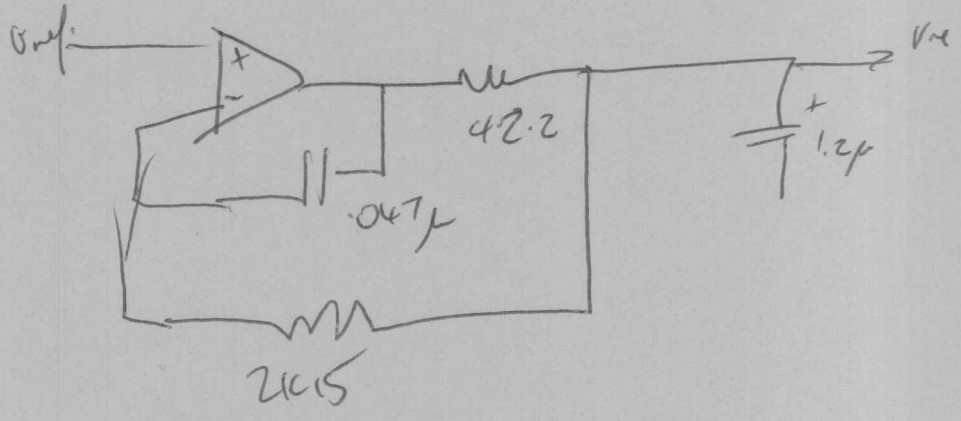


Appendix

Need More Information ?

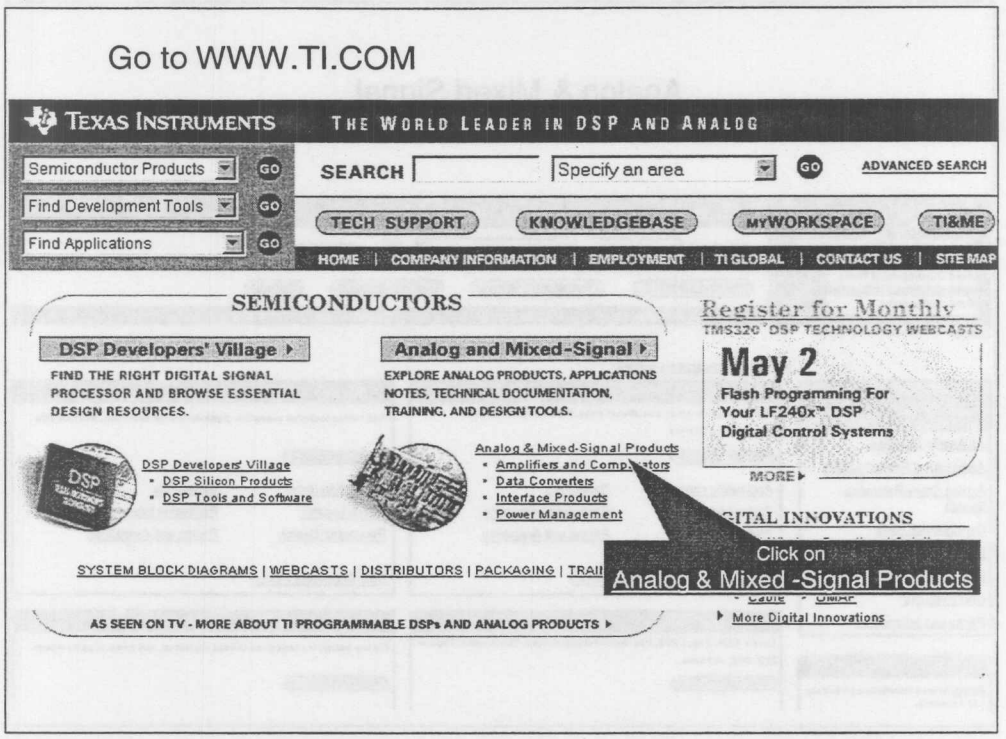
Additional Information About:

- Products
- Data Sheets
- Application Reports
- Evaluation Modules

Where:

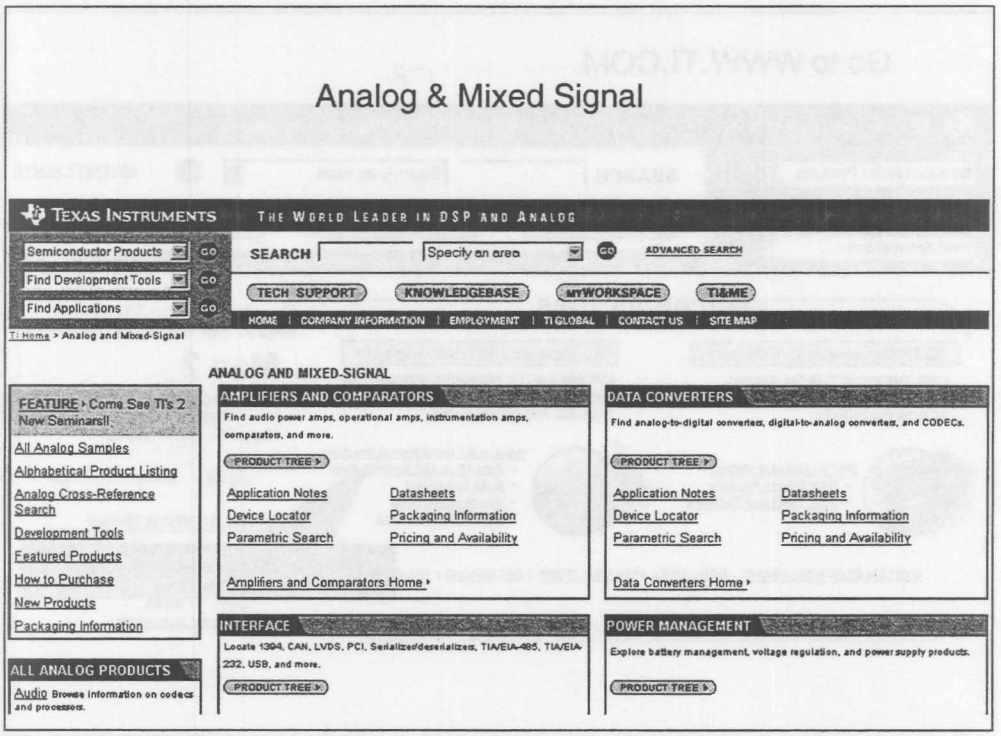
On the WWW at WWW.TI.COM

On the Phone at the TI Product Information Center



www.ti.com is the best place to start when looking for products and information from Texas Instruments. The home page contains links to product information as well as information about the company.

Selecting Analog & Mixed Signal Products links to the Analog and Mixed Signal home page.



This is the Analog & Mixed Signal Home Page.

From this page you can find products by their function (amplifier, DAC etc.) or part number. Data sheets, application reports, and evaluation modules can be found from the product page or by the literature number.

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